BAT32A6700 Datasheet

Ultra-low-power 32-bit microcontrollers based on ARM® Cortex®-M0+

Built-in 128K bytes Flash, integrated LDO, LIN transceiver, rich analog function, safety function, timer and various communication interfaces

V0.1.3 Draft Version

Feature

- **Ultra-low power operation environment:**
  - Supply voltage range: 5.5V to 28V
  - Temperature range: -40˚C to 125˚C
  - Low power modes: sleep mode, deep sleep mode
  - Operating power consumption: 120uA/MHz@48MHz
  - Power consumption in deep sleep mode: 42uA
  - Operation in deep sleep mode +32.768K+RTC: 45uA
- **Core:**
  - ARM®32-bit Cortex®-M0+ CPU with MPU memory protection unit and MTB on-chip tracking unit
  - Operating frequency: 32KHz to 48MHz
- **Memory:**
  - 128KB Flash memory with shared program and data storage
  - 1.5KB dedicated data Flash memory
  - 12KB SRAM Memory with parity check
- **Power and reset management:**
  - Built-in power-on reset (POR) circuit
  - Built-in voltage detection (LVD) circuit (settable threshold voltage)
- **Clock management:**
  - Built-in a high-speed oscillator with accuracy of ±1%, supporting 1MHz to 48MHz system clocks, and 1MHz to 64MHz peripheral module operation clocks
  - Built-in 15KHz low-speed oscillator
  - Support 1MHz~20MHz external crystal oscillators
  - Support 32.768KHz external crystal oscillators
- **Multiplier/divider module:**
  - Multiplier: Support single-cycle 32-bit multiplication operations
  - Divider: Support 32-bit signed integer division operations, only 4 or 8 CPU clock cycles to complete an operation
  - Comparator (CMP), built-in two-channel comparator, input source selectable, reference voltage selectable from external reference voltage or internal reference voltage
  - Programmable Gain Amplifier (PGA), built-in 2-channel PGA, programmable 4/8/10/12/14/16/32x gain, with external GND pin (can be used in differential mode)
- **Input/output ports:**
  - I/O ports: 41
  - It can switch between N-channel open drain, TTL input buffering, and internal pull-up
  - Key interrupt detection function
  - Controller for built-in clock output/buzzer output
- **Serial two-wire debugger (SWD)**
- **Rich timers:**
  - 16-bit timer: 9 channels (with general-purpose PWM and motor-specific PWM functions)
  - 15-bit interval timer: 1x
  - Real Time Clock (RTC): 1x (with perpetual calendar, alarm function, and support a wide range of clock correction)
  - Watchdog timer (WWDT): 1x
  - SysTick timer
- **Rich and flexible interfaces:**
  - 2 serial communication units: Serial communication unit 0 can be freely configured as 2-channel standard UART or 4-channel 3-wire SPI or 4-channel simplified I^2C; Serial communication unit 1 can be freely configured as 1-channel standard UART or 2-channel 3-wire SPI or 2-channel simplified I^2C; (Among them, the UART of unit 0 supports LIN-Bus communication, and the SPI00 channel supports 4-wire SPI communication)
  - Standard I^2C: 1 channel
  - IrDA: 1 channel
  - CAN: 1 channel
- **Integrated LIN transceiver compliant with LIN 2.x/ SAE J2602 protocol specifications**

- **Enhanced DMA controller:**
  - Interrupt trigger start
  - Selectable transfer modes (normal transfer mode, repeat transfer mode, block transfer mode and chain transfer mode)
  - Transfer source/destination realm are selectable from the full address space range
- **Linkage controller:**
  - It can link event signals to realize the linkage of peripheral functions
  - 22 input events and 10 trigger events
- **Rich analog peripherals:**
  - 12-bit ADC converter with 1.06Msps conversion rate, 15 external analog channels with temperature sensor(s) supporting for single-channel conversion mode and multi-channel scan conversion mode. Conversion range: 0 to positive V_{REF}
  - 8-bit D/A converter, 2-channel analog output, real-time output function, output voltage range: 0~VDD
- **Integrated 5V LDO to power internal MCU and external devices, input voltage range: 5.5 to 28V**
- **Safety function:**
  - Comply with IEC/UL 60730 standards
  - Report abnormal storage access errors
  - Support RAM parity check
  - Support CRC
  - Support SFR guard and avoid misoperation
  - 128-bit unique ID number
  - Flash Level 2 protection in the debug mode (Level1: only perform flash full-scale erase, cannot be read or written. Level2: Emulator connection is invalid, cannot operate on flash.)
- **Package:**
  - QFN48

1 Overview

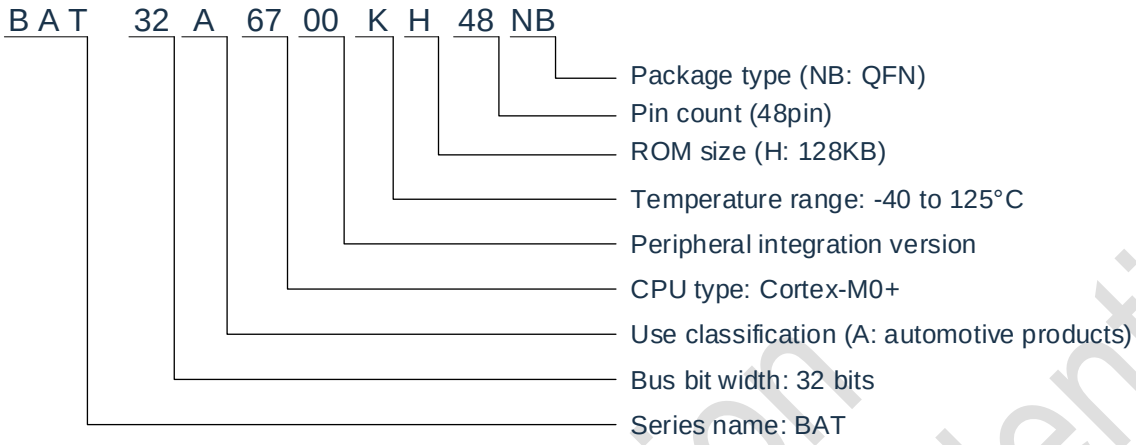
1.1 Brief introduction

The BAT32A6700 series complies with AEC-Q100 Grade 1 automotive product standards, operating in environments from -40 to 125°C. It supports a 48-pin QFN package. This product features a high-performance ARM®Cortex®-M0+ core, capable of operating up to 48MHz, with high-speed embedded flash (up to 128KB for program/data storage) and a maximum SRAM of 12KB. It integrates multiple standard interfaces including I^2C, SPI, UART, LIN, and CAN bus. Additionally, it includes a 12-bit A/D converter for sensor signal acquisition, reducing system design costs, an 8-bit D/A converter for audio playback or power control, a comparator and a programmable gain amplifier. The integrated temperature sensor monitors external environmental temperatures in real-time. The internal comparator can be used for motor control feedback or battery monitoring applications. The chip features advanced timer modules: 1 SysTick timer, 17 channels of 16-bit timers, 1 channel of 15-bit interval timer, watchdog timer, and real-time clock, supporting general-purpose PWM and motor-specific PWM functions.

The BAT32A6700 excels in low-power performance, supporting sleep and deep sleep modes with flexible design. It operates at 120uA/MHz @ 48MHz and consumes only 42uA in deep sleep mode. Featuring an integrated event link controller, it enables direct hardware module connection without CPU intervention, providing faster response times compared to interrupt-driven systems.

Integrated with LDO and LIN transceiver, the BAT32A6700 ensures excellent reliability, rich peripheral integration, and outstanding low-power performance, making it ideal for automotive electronics applications such as switches, doors, windows, lights, sensors, and motors.

1.2 Product model list



BAT32A6700 product list:

Product model	Flash memory	Dedicated data Flash memory	SRAM	Package
BAT32A6700KH48NB	128KB	1.5KB	12KB	48-pin plastic package QFN (6x6mm,0.4mm pitch)

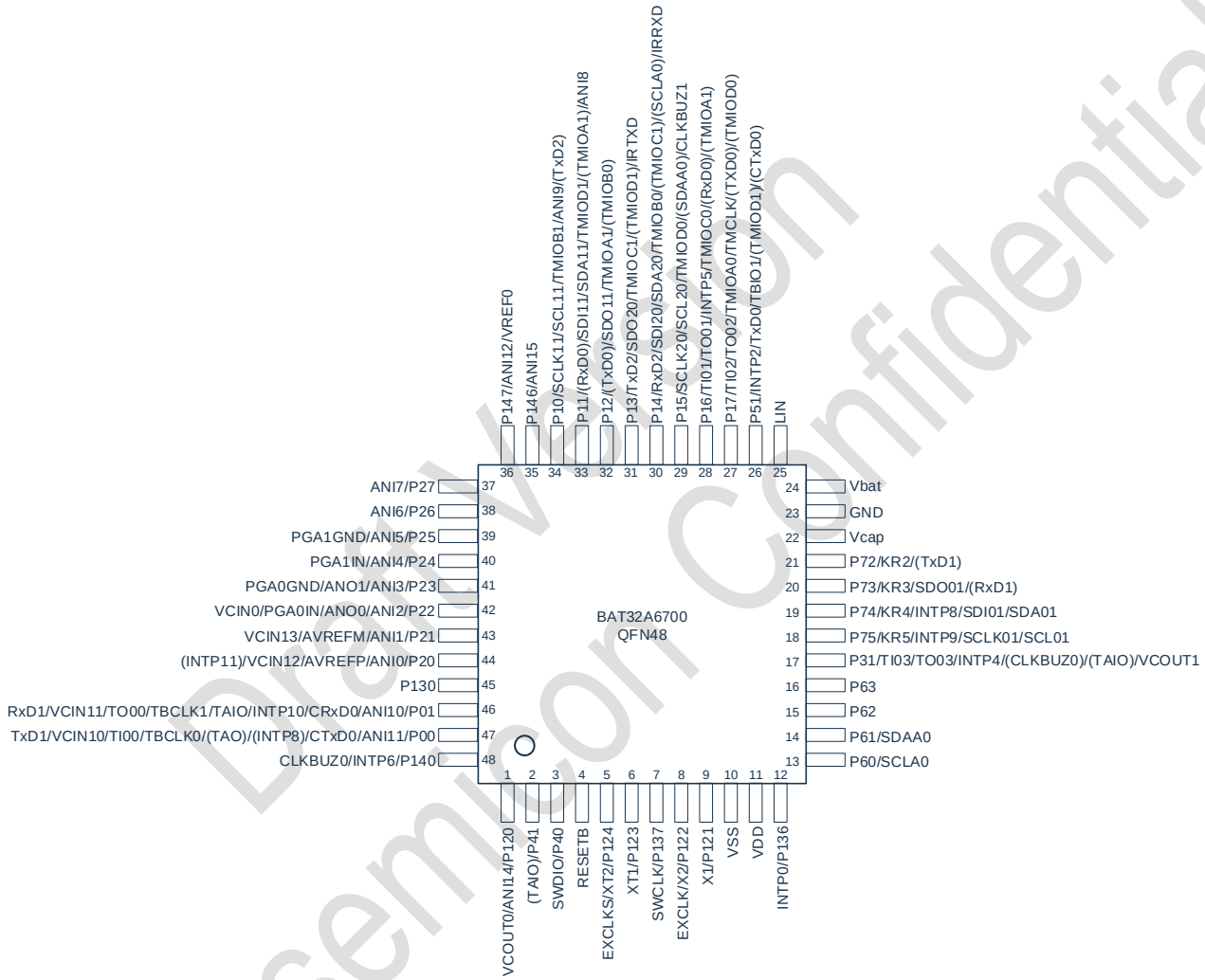
BAT32A6700 product list:

Part No.	Core	Clock frequency (MHz)	Internal LDO input (V)	MCU operating voltage (V)	Code Flash (KB)	SRAM (KB)	Data Flash (KB)	DMA	GPIO	12bit ADC	8bit DAC	CMP	PGA	Universal timer (16-bit)	RTC	WDT	UART	SPI	IIC bus	IrDA bus	LIN bus (integrated transceiver)	CAN bus	Hardware multiplier	Hardware divider	Package
BAT32A6700 KH48NB	M0+	48	5.5~28	5.0	128	12	1.5	36	41	15+4	2	2	2	9	1	1	3	3	1+3	1	1	1	Y	Y	QFN 48

1.3 Top view

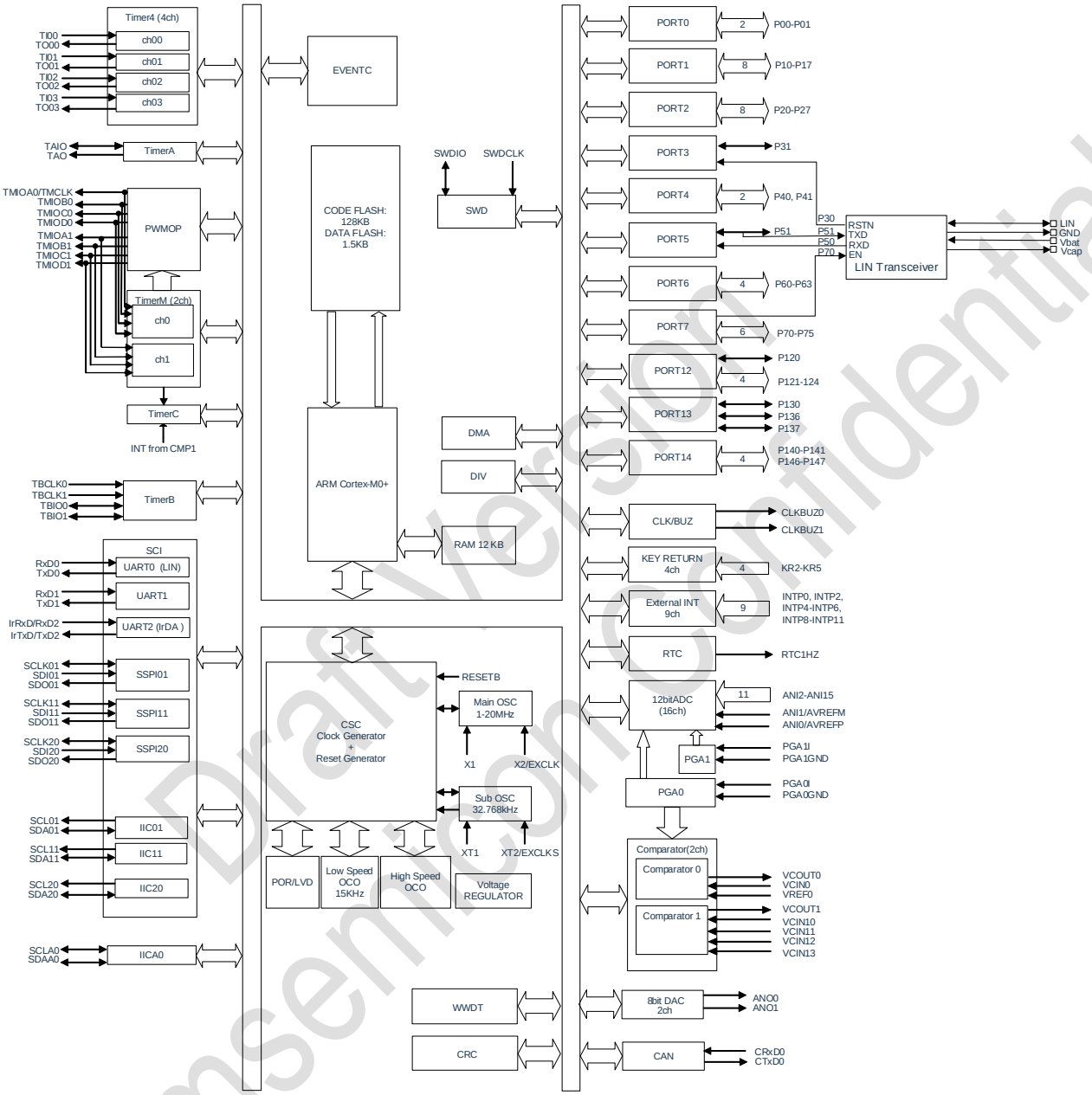
1.3.1 BAT32A6700KH48NB

- 48-pin plastic package QFN (6x6mm, 0.4mm pitch)

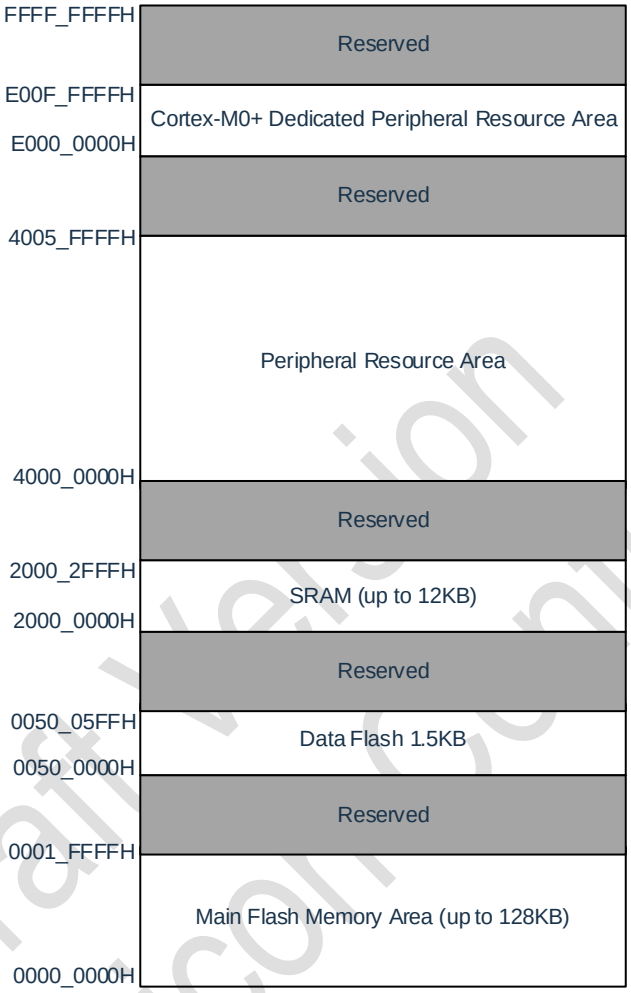


Remark: The functions shown in the above figure () can be assigned by setting the peripheral I/O redirection registers.

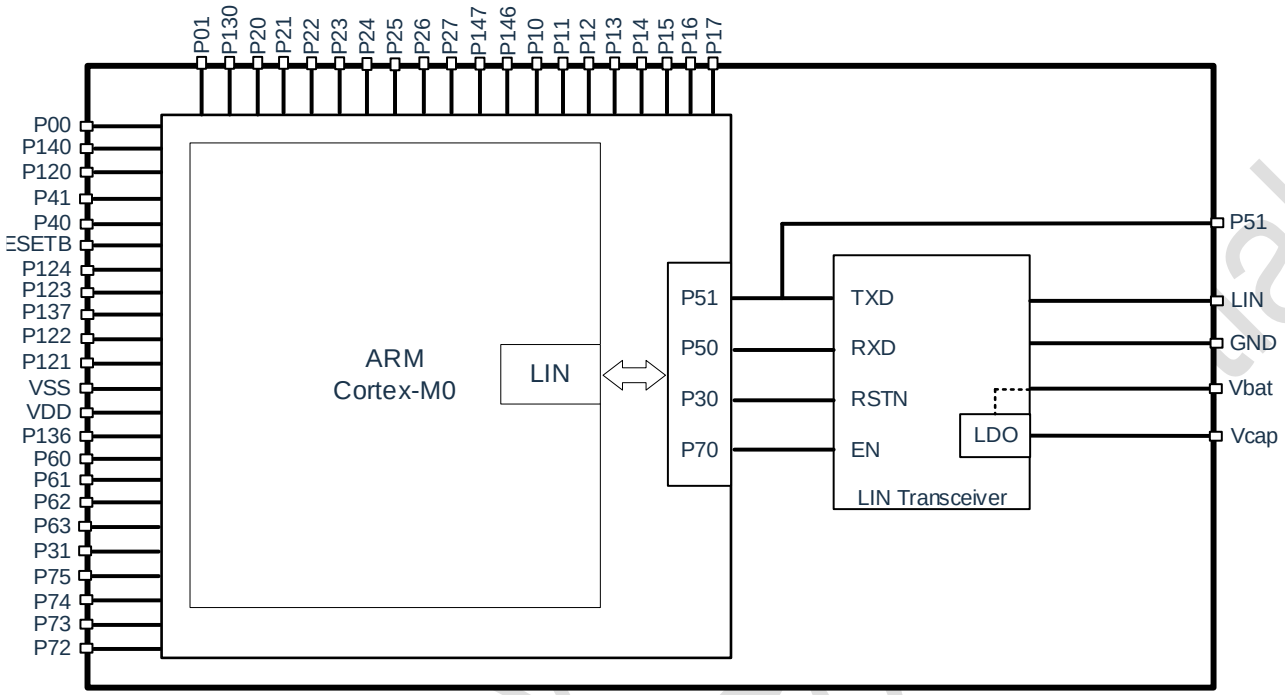
2 Product Structure Diagram



3 Memory Map



4 System Block Diagram



5 Pin Function

5.1 Port function

All ports of this product are divided into 6 types according to type, which are type1~type6, and the corresponding situations are as follows:

Type 1: Bidirectional I/O function

Type 2: NOD function, corresponding to pins P60-P63

Type 3: Input only function, e.g. clock, corresponding to pins P121-P124

Type 4: Output only function, corresponding to pin P130

Type 5: RESET function, corresponding to pin RESETB

Type 6: Other functions such as LIN, VSS/GND, VDD, Vcap.

See 5.3 Port Types for details of each type of pin block diagram.

5.1.1 48-pin products description

Name	Type	I/O	After the reset is released	Multplexing function	Function
P00	Type1	I/O	Analog function	ANI11/TxD1/VCIN10/TI00/TBCLK0/(TAO)/(INTP8)/CTxD0	Port 0 A 2-bit input/output port, can be designated as an input or output in bit units. Inputs can be set by software using internal pull-up resistors. The input of P01 can be set as the TTL input buffer. The P00 output can be set as the N-channel open drain output (V_{DD} withstand voltage). P00 and P01 can be set as analog inputs.
P01				ANI10/RxD1/VCIN11/TO00/TBCLK1/TAIO/INTP10/CRxD0	
P10		I/O	Analog function	SCLK11/SCL11/TMIOB1/ANI9/(TxD2)	Port 1 An 8-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors. The inputs of P10, P14~P17 can be set as TTL input buffers. The outputs of P10, P11, P13~P15 and P17 can be set as N-channel open drain outputs (V_{DD} withstand voltage). P10 and P11 can be set as analog inputs.
P11				(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12			Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)	
P13				TxD2/SDO20/TMIOC1/(TMIOD1)/IrTxD	
P14				RxD2/SDI20/SDA20/TMIOB0/(TMIOC1)/(SCLA0)/IrRxD	
P15				SCLK20/SCL20/TMIOD0/(SDAA0)/CLKBUZ1	
P16				TI01/TO01/INTP5/TMIOC0/(RxD0)/(TMIOA1)	
P17				TI02/TO02/TMIOA0/TMCLK0/TxD0)/(TMIOD0)	
P20		I/O	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2 An 8-bit input/output port, can be designated as an input or output in bit units. Can be set as an analog input.
P21				ANI1/AVREFM/VCIN13	
P22				ANI2/ANO0/PGA0IN/VCIN0	
P23				ANI3/ANO1/PGA0GND	
P24				ANI4/PGA1IN	
P25				ANI5/PGA1GND	
P26				ANI6	
P27				ANI7	
P31		I/O	Input port	TI03/TO03/INTP4/(CLKBUZ0)/(TAIO)/VCOUT1	Port 3 An input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
P40		I/O	Input port	SWDIO	Port 4 An input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
P41				(TAIO)	

P51	Type1	I/O	Input port	INTP2/ TxD0/TBIO1/(TMIOD1)/ (CTxD0)	Port 5 A 2-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors. The output of P51 can be configured as N-channel open drain outputs (VDD withstand voltage). If the LIN function is used, P51 can not be used as other IO function, it just floats.
P60	Type2	I/O	Input port	SCLA0	Port 6 A 4-bit input/output port, can be designated as an input or output in bit units. The outputs of P60 to P63 can be set as N-channel open drain outputs (6V withstand voltage).
P61				SDAA0	
P62				—	
P63				—	
P72	Type1	I/O	Input port	KR2/(TxD1)	Port 7 A 6-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors. The output of P74 can be set as the N-channel open drain output (V_{DD} withstand voltage).
P73				KR3/SDO01/(RxD1)	
P74				KR4/INTP8/SDI01/SDA01	
P75				KR5/INTP9/SCLK01/SCL01	
P120		I/O	Analog function	ANI14/VCOUT0	Port 12 A 1-bit input/output port and a 4-bit input-only port. Only the P120 has output function. The input port can be set by software using internal pull-up resistors. P120 can be set as an analog input.
P121	Type3	I	Input port	X1	
P122				X2/EXCLK	
P123				XT1	
P124				XT2/EXCLKS	
P130	Type4	O	Output port	—	Port 13 A 1-bit output-only port and a 2-bit input/output port. P137 can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
P136	Type1	I/O	Input port	INTP0	
P137				SWCLK	
P140			Input port	CLKBUZ0/INTP6	Port 14 A 3-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors. P146 and P147 can be set as analog inputs.
P146			Analog function	ANI15	
P147				ANI12/VREF0	
RESETB	Type5	I	—	—	An input dedicated pin for external reset When the external reset is not used, it must be connected to VDD either directly or through a resistor.
LIN	Type6	I/O	LIN communication	—	A LIN bus input/output port
Vcap		Power supply	—	—	LDO output 5V, can provide power for internal MCU and external devices, with external 0.1uF + 10uF decoupling capacitor
VDD		Power supply	—	—	An MCU power input
Vbat		Power supply	—	—	Battery supply voltage
GND/VSS		Ground	—	—	Ground

Remark:

1. Each pin is set to digital or analog (capable of being set in bits) via Port Mode Control Register x (PMCx).

2. See “5.2 Port Multiplexing Function” for the description of the multiplexing function.
3. The functions in the above table () can be assigned by setting the peripheral I/O redirection registers.

5.2 Port multiplexing function

(1/2)

Name	I/O	Function
ANI0~ANI15	I	A/D converter analog inputs
ANO0,ANO1	O	D/A converter outputs
INTP0~INTP11	I	External interrupt request inputs Designation of active edges: rising edge, falling edge, double edge
VCIN0	I	Comparator 0 analog voltage inputs
VCIN10, VCIN11, VCIN12, VCIN13	I	Comparator 1 analog voltage/reference voltage inputs
VREF0	I	Comparator 0 reference voltage inputs
VCOUT0, VCOUT1	O	Comparator outputs
PGA0IN, PGA1IN	I	PGA inputs
PGA0GND, PGA1GND	I	PGA reference inputs
KR0~ KR7	I	Key interrupt inputs
CLKBUZ0, CLKBUZ1	O	Clock output/buzzer outputs
RTC1HZ	O	Correction clock (1Hz) output for real-time clock
RESETB	I	A system reset input that is active low and must be connected to V_{DD} either directly or through a resistor when an external reset is not used.
CRxD0	I	CAN serial data inputs
CTxD0	O	CAN serial data outputs
IrRxD	I	IrDA serial data inputs
IrTxD	O	IrDA serial data outputs
RxD0~RxD2	I	Serial data inputs of serial interfaces UART0, UART1 and UART2
TxD0~TxD2	O	Serial data outputs of serial interfaces UART0, UART1 and UART2
SCL01, SCL11, SCL20	O	Serial clock outputs of serial interfaces IIC01, IIC11 and IIC20
SDA01, SDA11, SDA20	I/O	Serial data inputs/outputs of serial interfaces IIC01, IIC11 and IIC20
SCLK01, SCLK11, SCLK20	I/O	Serial clock inputs/outputs of serial interfaces SSPI01, SSPI11 and SSPI20
SDI01, SDI11, SDI20	I	Serial data inputs of serial interfaces SSPI01, SSPI11 and SSPI20

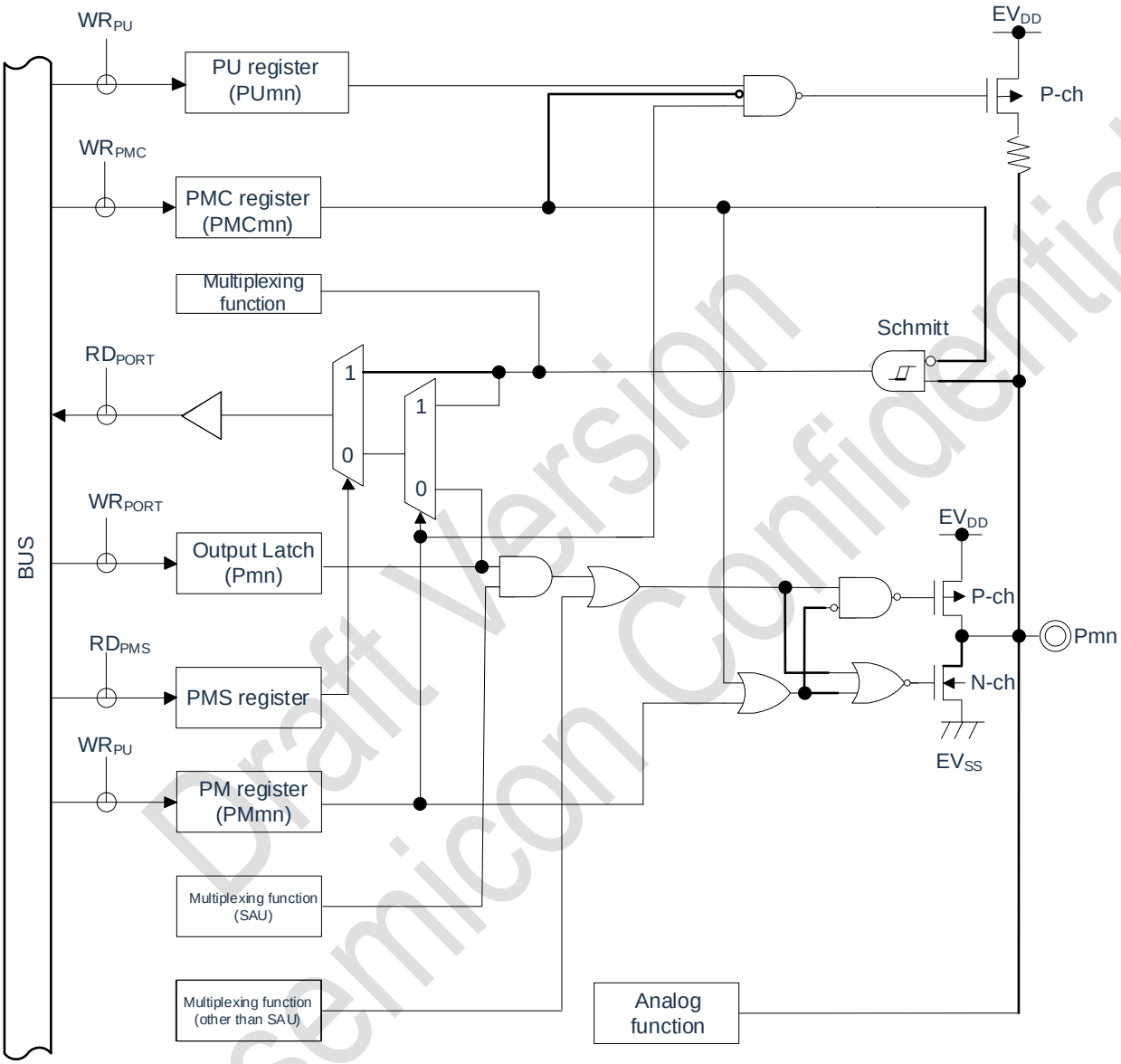
(2/2)

Name	I/O	Function
SDO01, SDO11, SDO20	O	Serial data outputs of SSPI01, SSPI11 and SSPI20
SCLA0	I/O	Clock inputs/outputs of serial interface IICA0
SDAA0	I/O	Serial data inputs/outputs of serial interface IICA0
TI00 ~TI03	I	External count clock/capture trigger inputs for 16-bit Timer4
TO00 ~TO03	O	Timer outputs for 16-bit Timer4
TAIO	I/O	TimerA inputs/outputs
TAO	O	TimerA outputs
TMCLK	I	External clock inputs for TimerM
TMIOA0, TMIOB0, TMIOC0, TMIOD0, TMIOA1, TMIOB1, TMIOC1, TMIOD1	I/O	TimerM inputs/outputs
TBIO0, TBIO1	I/O	TimerB inputs/outputs
TBCLK0, TBCLK1	I	External clock inputs for TimerB
X1, X2	—	Resonator for main system clock connection
EXCLK	I	External clock inputs for main system clock
XT1, XT2	—	Resonator for slave system clock connection
EXCLKS	I	External clock inputs for subsystem clock
AV_{REFP}	I	Positive (+) reference voltage inputs for A/D converter
AV_{REFM}	I	Negative (-) reference voltage inputs for A/D converter
SWDIO	I/O	SWD data interface
SWCLK	I	SWD clock interface
LIN	I/O	LIN bus input/output ports
V_{SS}	-	Power ground
GND	-	Power ground
Vbat	-	Battery supply voltage
Vcap	-	LDO Output - Provides power to internal MCU and external devices, requires external 0.1uF+10uF decoupling capacitors.
VDD	-	MCU power supply

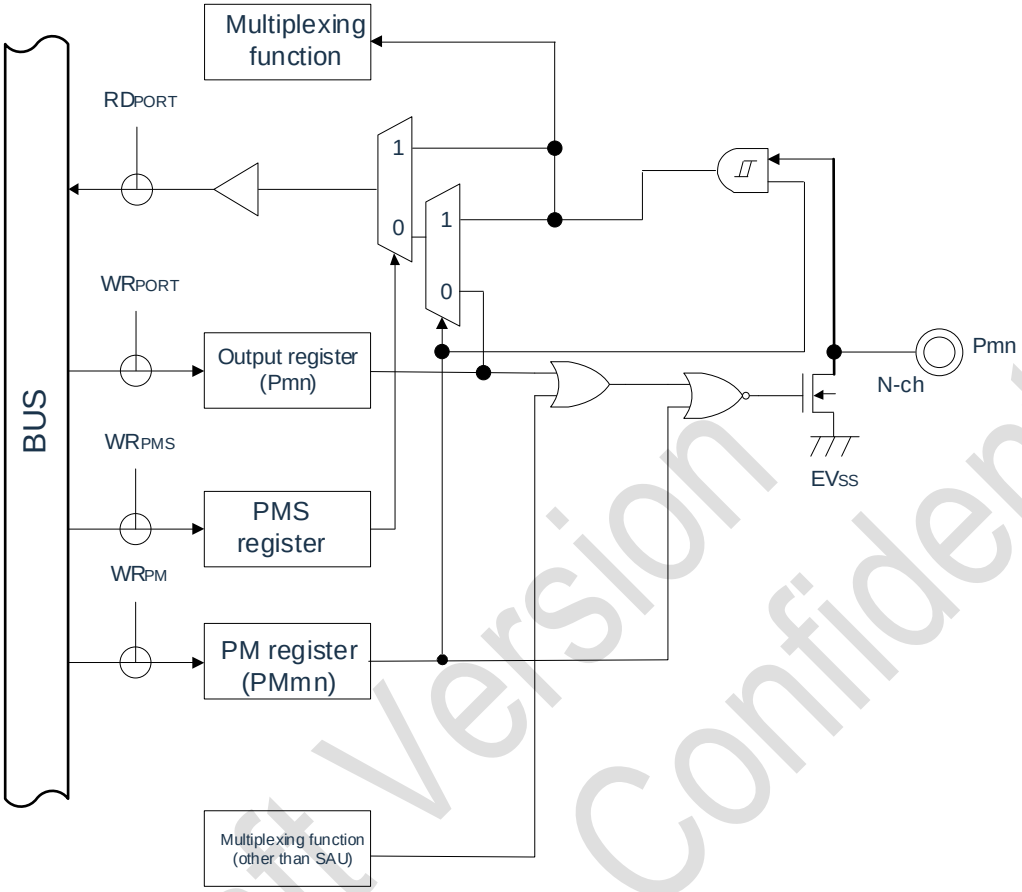
Remark: As a countermeasure against noise and lockup, a bypass capacitor (about 0.1uF) must be connected between VDD-V_{SS} and Vcap-V_{SS} at the shortest possible distance and with thicker wiring.

5.3 Port types

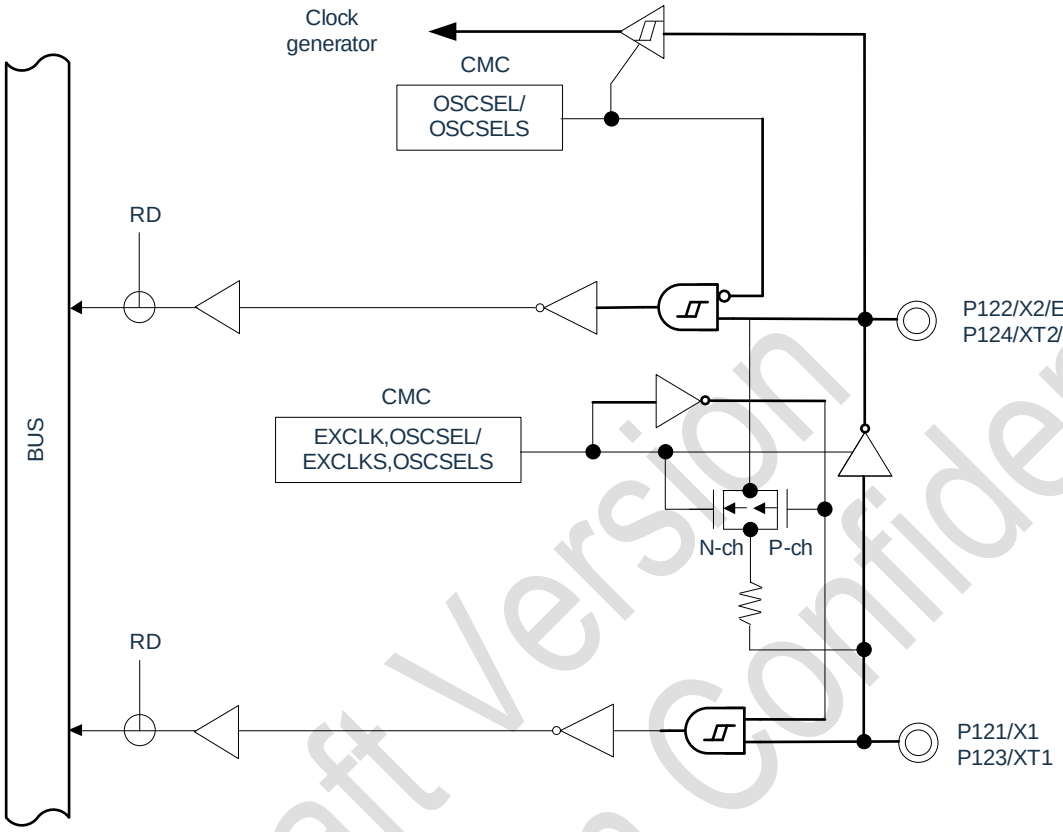
Type 1: Bidirectional I/O function



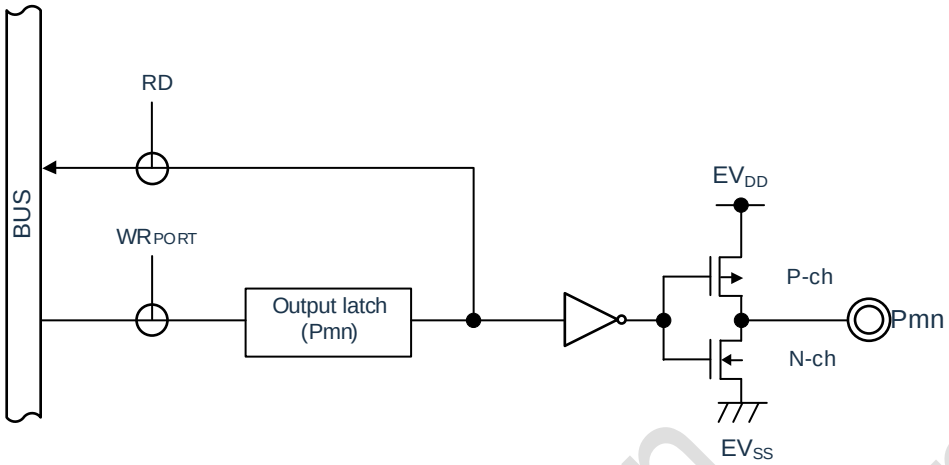
Type 2: NOD function



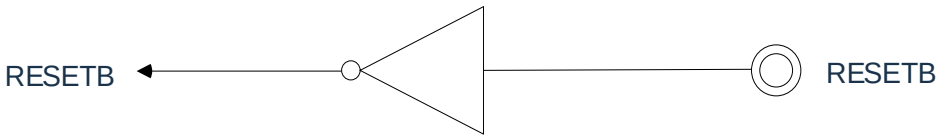
Type 3: Input-only function



Type 4: Output-only function



Type 5: RESET function



6 Function Summary

6.1 ARM® Cortex®-M0+ core

ARM Cortex-M0+ processor is the next generation of ARM processors for embedded systems. It provides a low-cost platform designed to meet the needs of low-pin-count and low-power microcontrollers while providing excellent computing performance and advanced system response to interrupts.

The Cortex-M0+ processor's 32-bit RISC processor provides superior code efficiency and delivers the high-performance expectations of an ARM core, unlike 8-bit and 16-bit devices of the same memory size. The Cortex-M0+ processor has 32 address lines and up to 4G of storage.

The BAT32A6700 uses an embedded ARM core, making it compatible with all ARM tools and software.

6.2 Memory

6.2.1 Flash memory

The BAT32A6700 has built-in flash memory that can be programmed, erased, and rewritten. It has the following functions:

- Programs and data share 128K storage.
- 1.5KB dedicated data Flash memory.
- Support page erasure, the size of each page is 512byte.
- Support byte/half-word/word (32bit) programming.

6.2.2 SRAM

The BAT32A6700 contains 12KB of embedded SRAM.

6.3 Enhanced DMA controller

It has a built-in enhanced DMA (Direct Memory Access) controller that enables data transfer between memories without using the CPU.

- DMA can be started via peripheral function interrupts, enabling real-time control through communication, timers, and A/D.
- The transfer source/target field is optional for the full address space range (when the flash field is used as the target address, flash needs to be preset as the programming mode).
- Support 4 modes (normal transfer mode, repeat transfer mode, block transfer mode and chain transfer mode).

6.4 LIN transceiver

BAT32A6700 is a System-on-Chip (SoC) product featuring an integrated LDO and serving as a local interconnect network (LIN) physical layer transceiver. Its internal LIN transceiver provides a stable 5V power supply for Electronic Control Units (ECUs), microcontrollers, or related peripherals. The LIN transceiver complies with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12V), and SAE J2602 standards. It is primarily designed for automotive networks operating at transmission rates from 1kbps to 20kbps. The transceiver's LIN bus output pins feature internal pull-up resistors and waveform shaping to reduce electromagnetic emissions (EME). It supports full-duplex communication, with the TXD pin for input to send low-voltage signals from the microcontroller to the LIN bus. Simultaneously, the LIN pin receives data streams from the bus, and the receiver's output pin RXD transmits data back to the microcontroller or to other microcontrollers.

The integrated internal LIN transceiver operates within a voltage range of 5.5V to 28V, suitable for 12V applications. In sleep mode, the transceiver achieves ultra-low current consumption, swiftly minimizing power consumption in case of faults. It supports remote wake-up via the LIN bus or normal operation mode activation via the EN pin. Additionally, it provides a power-on and power-down detection output pin RSTN for monitoring the status of the 5V regulator by the microcontroller.

6.5 Linkage controller

The linkage controller links the output events by each peripheral function with the peripheral function trigger sources. This enables collaborative operation between peripheral functions without using the CPU.

The linkage controller has the following functions:

- It can link event signals together to realize the linkage of peripheral functions.
- There are 22 types of event input and 10 types of event triggering.

6.6 Clock generation and startup

A clock generation circuit is a circuit that generates a clock to the CPU and peripheral hardware. There are three types of system clocks and clock oscillation circuits.

6.6.1 Main system clock

- X1 oscillation circuit: The resonator can be connected to pins (X1 and X2) to generate a clock oscillation of 1~20MHz, and the oscillation can be stopped by executing a deep sleep command or setting MSTOP.
- High-speed on-chip oscillator (high-speed OCO): Oscillation can be performed by selecting the frequency by the option byte. After released, the CPU starts running at this high-speed on-chip oscillator clock by default. Oscillation can be stopped by executing a deep sleep command or setting the HIOSTOP bit. The frequency set by the option byte can be changed through the frequency selection register of the high-speed on-chip oscillator. The maximum frequency is 64MHz with an accuracy ±1.0%.
- Input external clock from pin (X2): (1~20MHz), and the input of the external main system clock can be invalidated by executing a deep sleep command or setting the MSTOP bit.

6.6.2 Subsystem clock

- XT1 oscillator circuit: A 32.768kHz clock oscillation can be generated by connecting a 32.768kHz resonator to the pins (XT1 and XT2), and the oscillation can be stopped by setting the XTSTOP bit.
- An external clock input by the pin (XT2): 32.768kHz, and the external clock input can be disabled by setting the XTSTOP bit.

6.6.3 Low-speed on-chip oscillator clock

Low-speed on-chip oscillator (low-speed OCO): generate a 15kHz (TYP.) clock oscillation. The low-speed on-chip oscillator clock cannot be used as the CPU clock. Only the following peripheral hardware can run off the low-speed on-chip oscillator clock.

- Watchdog timer (WWDT)
- Real time clock (RTC)
- 15-bit interval timer
- TimerA

6.7 Power management

6.7.1 Power supply mode

Vbat: Battery supply voltage, voltage range: 5.5V~28V, support 12V system;

Vcap: LDO output voltage 5V, voltage range: 4.9V~5.1V, must be connected with 0.1uF and 10uF filter capacitor.

VDD: MCU input voltage, voltage range: 2.0V~5.5V (in practice, Vcap will be connected to VDD, no need to supply additional power to MCU).

6.7.2 Power-on reset

The power-on reset circuit (POR) has the following functions.

- An internal reset signal is generated when power is applied. If the MCU voltage (V_{DD}) is greater than the detection voltage (V_{POR}), the reset is released. However, the reset state must be maintained by a voltage detection circuit or an external reset until the operating voltage range is reached.
- Compare the MCU voltage (V_{DD}) and the detection voltage (V_{POR}), when $V_{DD} < V_{POR}$, an internal reset signal is generated. However, when the power supply drops, it must be shifted to the deep sleep mode or set to the reset state by the voltage detection circuit or external reset before falling below the operating voltage range. If operation is to be restarted, it must be verified that the power supply voltage has returned to within the operating voltage range.

6.7.3 Voltage detection

The voltage detection circuit sets the operating mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) via option bytes. The voltage detection (LVD) circuit has the following functions:

- Compare the MCU voltage (V_{DD}) and the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) and generate an internal reset or interrupt request signal.
- The detection voltage of the MCU voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected by the option bytes.
- Can run in deep sleep mode.
- When the power supply rises, it must be maintained in the reset state by voltage detection circuit or an external reset before reaching the operating voltage range. When the power supply drops, it must be switched to deep sleep mode before it is less than the operating voltage range, or set to reset by voltage detection circuit or external reset.
- The operating voltage range varies depending on the setting of the user option bytes.

6.8 Low-power mode

The BAT32A6700 supports two low-power modes to achieve the best compromise between low power consumption, short start-up time, and available wake-up sources:

- Sleep mode: Sleep mode is entered by executing the sleep instruction. Sleep mode is a mode to stop the CPU running clock. If the high-speed system clock oscillator circuit or the high-speed on-chip oscillator is oscillating before the sleep mode is set, each clock continues to oscillate. Although this mode does not allow the operating current to be reduced to the level of deep sleep mode, it is an effective mode when processing is to be restarted immediately by an interrupt request or when frequent intermittent operation is to be performed.
- Deep sleep mode: Deep sleep mode is entered by executing the deep sleep instruction. Deep sleep mode is a mode that stops the oscillation of the high-speed system clock oscillator and high-speed on-chip oscillator and stops the whole system. The operating current of the chip can be greatly reduced. Since the deep sleep mode can be canceled by an interrupt request, intermittent operation is also possible. However, in the case of the X1 clock, since it is necessary to wait for the oscillation to stabilize when releasing the deep sleep mode, it is necessary to select the sleep mode if it is necessary to start processing immediately by an interrupt request.

In any of these modes, the registers, flags, and data memories remain as they were before being set to standby mode, and the status of the output latches and output buffers of the input/output ports is also maintained.

6.9 Reset function

The following seven methods generate a reset signal.

(1) An external reset is input via the RESETB pin.
(2) The program utilizes watchdog timers for internal reset as a means of detecting and responding to program instability.
(3) An internal reset is generated by comparing the supply voltage and the detection voltage of the power-on reset (POR) circuit.
(4) An internal reset is generated by comparing the supply voltage and the detection voltage of the voltage detection circuit (LVD).
(5) An internal reset occurs due to a RAM parity error.
(6) An internal reset occurred due to access to illegal memory.
(7) Software reset

The internal reset is the same as the external reset, and after the reset signal is generated, the procedure is executed from the addresses written in addresses 0000H and 0001H.

6.10 Interrupt function

The Cortex-M0+ processor has a built-in Nested Vector Interrupt Controller (NVIC) that supports up to 32 interrupt request (IRQ) inputs, a non-maskable interrupt (NMI) input, and multiple internal exceptions.

This product expands 32 maskable interrupt requests (IRQ) and 1 non-maskable interrupt (NMI) to support up to 64 maskable interrupt sources and one non-maskable interrupt source. The actual number of interrupt sources varies by product.

		48 pins
Maskable interrupt	External	11
	Internal	29

6.11 Real-time clock (RTC)

Functions of real-time clock (RTC) are show as below.

- Holds counters for years, months, weeks, days, hours, minutes, and seconds
- Fixed cycle break (cycles: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm clock interrupt (alarm clock: week, hour, minute)
- 1Hz pin out capability
- Support prescalers of subsystem clock or main system clock as RTC operation clocks.
- Real-time clock interrupt signals (INTRTC) can be used to wake up in deep sleep mode.
- Watch error correction with high accuracy

Year, month, week, day, hour, minute and second counters are only available if the subsystem clock (32.768kHz) or main system clock prescaler is selected as the RTC operation clock. When the low-speed on-chip oscillator clock (15kHz) is selected, only the fixed-cycle interrupt function can be used.

6.12 Watchdog timer

The 1- channel WWDT and 17-bit watchdog timer operation are set by option byte count. The watchdog timer operates on a low-speed on-chip oscillator clock (15KHz). The watchdog timer is used to detect program instability. When program instability is detected, an internal reset signal is generated.

The following are judged to be program instability:

- When the watchdog timer counter overflows
- When a bit operation instruction is executed on the watchdog timer enable register (WDTE)
- When writing data other than “ACH” to the WDTE register
- When writing data to the WDTE register during window closure

6.13 SysTick timer

This timer is exclusive to real-time operating systems, but can also be used as a standard decrement counter.

It is characterized by the generation of a maskable system interrupt when the 24-bit decrementing counter self-loading capacity counter reaches zero.

6.14 Timer4

The Timer4 is a built-in timer unit containing four 16-bit timers, each of which is called a “channel” and can be used as an independent timer or in combination with multiple channels for advanced timer functions.

For details of each function, refer to the table below.

Independent channel operation function	Multi-channel linkage operation function
● Interval timer ● Square wave output ● External event counter ● Frequency divider ● Input pulse interval measurement ● Input signal high/low width measurement ● Delay counter	● Single trigger pulse output ● PWM output ● Multiple PWM output

6.14.1 Independent channel operation function

The independent channel operation function is a function that allows you to use any channel independently of other channel operation modes. The independent channel operation function is used in the following modes:

(1) Interval timer: It can be used as a reference timer for generating interrupts at fixed intervals (INTTM).

(2) Square wave output: Whenever an INTTM interrupt is generated, a flip is triggered to output a 50% duty cycle square wave from the timer output pin (TO).

(3) External event counter: Count the effective edge of the input signal of the timer input pin (TI) and can be used as an event counter to generate an interrupt if the specified number of times is reached.

(4) Divider function (limited to channel 0 of unit 0): divide the input clock of the timer input pin (TI00) and output it from the output pin (TO00).

(5) Measurement of input pulse interval: The interval between input pulses is measured by starting counting at the effective edge of the input pulse signal at the timer input pin (TI) and capturing the count value at the effective edge of the next pulse.

(6) High/low width measurement of input signal: Measure the high or low width of the input signal by starting counting on one edge of the input signal of the timer input pin (TI) and capturing the count value on the other edge.

(7) Delay counter: Starts counting at the effective edge of the input signal at the timer input pin (TI) and generates an interrupt after an arbitrary delay period has elapsed.

6.14.2 Multi-channel linkage operation function

The multi-channel linkage operation function is a function that combines the master channel (the reference timer for the main control period) and the slave channel (the timer that follows the operation of the master channel). The multi-channel linkage function can be used in the following modes:

1) Single trigger pulse output: Two channels are used in pairs to generate a single trigger pulse that can arbitrarily set the output timing and pulse width.
2) PWM (Pulse Width Modulation) output: Two channels are used in pairs to generate pulses that can set the period and duty cycle arbitrarily.
3) Multiple PWM (Pulse Width Modulation) output: Up to 3 PWM signals of any duty cycle can be generated at a fixed period by expanding the PWM function and using one master channel and multiple slave channels.

6.14.3 8-bit timer operation function

The 8-bit timer operation function uses the 16-bit timer channel as the function of two 8-bit timer channels. (Only Channel 1 and Channel 3 can be used).

6.14.4 LIN-bus support function

The Timer4 unit can be used to check whether the received signal in the LIN-bus communication is suitable for the LIN-bus communication format.

1) Wake-up signal detection: The low-level width is measured by starting counting on the falling edge of the input signal on the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the low width is greater than or equal to a fixed value, it is considered a wake-up signal.
2) Detection of the break field: After a wake-up signal is detected, the low-level width is measured by starting counting from the falling edge of the input signal of the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the width of the low level is greater than or equal to a fixed value, it is considered to be a break field.
3) Measurement of sync field pulse width: After detecting the break field, measure the low- and high-level widths of the input signal of the UART serial data input pin (RxD). The baud rate is calculated from the bit interval of the synchronization field measured in this way.

6.15 TimerA

This product has a built-in 16-bit TimerA, consisting of a reload register and a decrement counter. Available for the following operating modes:

- Timer mode: Count the counting source (the counting source can be a clock or an external event)
- Pulse output mode: Count the counting source and output a pulse when overflowing
- Event counting mode: Count external events and works in deep sleep mode.
- Pulse width measurement mode: Measurement of external pulse width
- Pulse period measurement mode: Measurement of external pulse period

6.16 TimerM

This product has a built-in 2-channel 16-bit TimerM optimized for motor control, which has the following 4 operating modes:

- Timer mode:
  - Input capture function (external signal as trigger, count value to register)
  - Output comparison function (detect whether the count value and register value are the same, and can change the output of the pin during detection)
  - PWM function (continuous output of arbitrary pulse width)
- Reset synchronous PWM mode: output sawtooth wave modulation, three-phase waveforms (6) without dead time
- Complementary PWM mode: output triangle wave modulation, three-phase waveforms (6) with dead time
- PWM3 mode: Output same-cycle PWM waveforms (2)

6.17 TimerB

This product has a built-in 16-bit TimerB, which has the following 3 modes:

- Timer mode:
  - Input capture function counts on both sides of the rising edge, falling edge, or rising/ falling edge.
  - Output compare function “L” level output, “H” level output or alternating output
- PWM mode: Can perform PWM output with arbitrary duty cycle.
- Phase counting mode: The counting value of the 2-phase encoder can be measured automatically.

6.18 TimerC

This product has a built-in 16-bit TimerC, which can be triggered by software, comparator or TimerM to realize the input capture function.

6.19 15-bit interval timer

This product has a built-in 15-bit interval timer that generates interrupts (INTIT) at any pre-set time interval, which can be used to wake up from deep sleep mode.

6.20 Clock output/buzzer output controller

The clock output controller is used to provide the clock to the peripheral IC, and the buzzer output controller is used to output the square wave of the buzzer frequency. The clock output or buzzer output is realized by dedicated pins.

6.21 Universal serial communication unit

This product has two built-in general-purpose serial communication units, each with up to four serial communication channels. It can realize standard SPI, simplified SPI, UART and simplifed I^2C communication. The functions of each channel are assigned as follows.

6.21.1 3-wire serial interface (SSPI)

Data is transmitted and received synchronously with the serial clock (SCK) output of the master device.

This is a clock-synchronous communication interface that communicates using a total of three communication lines: one serial clock (SCK), one transmit serial data (SO), and one receive serial data (SI).

[Data transmission and reception]

- Data length of 7 or 8 bits
- Phase control of data transmission and reception
- MSB/LSB first

[Clock control]

- Master or slave selection
- Phase control of input/output clock
- Transfer cycles generated by prescalers and channel internal counters
- Maximum transfer rate

  Master communication: Max. $F_{CLK}/2$

  Slave communication: Max. $F_{MCK}/6$

[Interrupt function]

- Transfer end interrupt, buffer null interrupt

[Error detection flag]

- Overflow error

6.21.2 SPI with slave chip selection

This is a clock-synchronous communication interface that communicates using a slave chip select input (SSI), a serial clock (SCK), a transmit serial data (SO), and a receive serial data (SI) for a total of four communication lines.

[Data transmission and reception]

- Data length of 7 or 8 bits
- Phase control of data transmission and reception
- MSB/LSB first
- Level settings of transmit and receive data

[Clock control]

- Phase control of input/output clocks
- Transfer cycles generated by prescalers and channel internal counters
- Maximum transfer rate

  Slave communication: Max. $F_{MCK}/6$

[Interrupt function]

- Transfer end interrupt, buffer null interrupt

[Error detection flag]

- Overflow error

6.21.3 UART

This function enables asynchronous communication over two lines, serial data transmission (TxD) and serial data reception (RxD). Using these two communication lines, data is transmitted and received asynchronously (using the internal baud rate) with other communicating parties in the data frame (consisting of start bits, data, parity bits, and stop bits). Full-duplex UART communication can be implemented by using two channels, dedicated transmitting (even channels) and dedicated receiving (odd channels), and LIN-bus can also be supported by combining a Timer4 unit and an external interrupt (INTP0).

[Data transmission and reception]

- Data length of 7, 8, or 9 bits
- MSB/LSB first
- Level setting for transmitting and receiving data, selection of inversion
- Parity bit appending, parity check function
- Stop bit appending, stop bit detection

[Interrupt function]

- Transfer end interrupt, buffer null interrupt
- Error interrupts caused by frame errors, parity check errors, or overflow errors

[Error detection flag]

- Frame errors, parity errors, overflow errors

[LIN-bus function].

- Detection of wake-up signals
- Detection of break fields (BF)
- Measurement of synchronous fields, calculation of baud rate

6.21.4 Simplified I²C

It is a function to synchronize clock communication with multiple devices through two lines of serial clock (SCL) and serial data (SDA). Since this simplified I²C is designed for single communication with devices such as Flash memory, and A/D converters, it is used only as a master device. The start and stop conditions, like the operation control registers, must comply with the AC characteristics and are handled by the software.

[Data transmission and reception]

- Master transmission, master reception (limited to the master function of single master)
- ACK output function, ACK detection function
- 8-bit data length (when transmitting the addresses, specify the addresses with the highest 7 bits, and use the lowest bit for R/W control)
- Start and stop conditions are generated by software

[Interrupt function]

- Transfer end interruption

[Error detection flag]

- ACK error, overflow error

[Simplified I²C unsupported features]

- Slave transmission, slave reception
- Multi-master function (arbitration failure detection function)
- Wait detection function

6.22 Standard serial interface IICA

This product is equipped with a serial interface IICA, supports slave dual address, and has the following three modes.

(1) Run-stop mode

This is the mode used when serial transfer is not performed, which reduces power consumption.

(2) I^2C bus mode (support multi-master)

This mode transmits 8-bit data to multiple devices over 2 wires of a serial clock (SCLA) and a serial data bus (SDAA). In accordance with the I^2C bus format, the master device can generate “start conditions”, “address”, “indication of transmission direction”, “data” and “stop conditions” on the serial data bus for the slave devices. The slave device automatically detects the received status and data by hardware. This feature simplifies the I^2C bus control part of the application program. Since the SCLA and SDAA pins of the serial interface IICA are used as open drain outputs, pull-up resistors are required for the serial clock line and the serial data bus.

(3) Wake-up mode

In deep sleep mode, when an extension code or a local station address is received from the master device, the deep sleep mode can be released by generating an interrupt request signal (INTIICA). This is set via the IICA control register.

6.23 Controller CAN

Universal CAN controller interface function, conforms to the standard CAN protocol in ISO 11898.

- Conform to ISO 11898 and is tested according to ISO/DIS 16845 (CAN compliance).
- Use standard and extended frames for reception and transmission.
- Communication speed: Max. 1Mbps (CAN input clock is equal to or greater than 8MHz)
- Each channel has 16 message buffers.
- Receive/transmit history list function.
- Automatic block transfer function.
- Multi-buffer receive block function.
- Mask settings for four modes per channel.

6.24 Analog-to-digital converter (ADC)

This product has a built-in 12-bit resolution analog-to-digital converter, SARADC, which converts analog inputs to digital values and controls the A/D conversion of up to 15 analog channels (ANI0~ANI12, ANI14~ANI15). The ADC contains the following functions:

- 12-bit resolution, slew rate: 1.06Msps.
- Triggering mode: support software triggering, hardware triggering and hardware triggering in standby state.
- Channel selection: support single-channel select mode and multi-channel scan mode.
- Conversion mode: support single conversion and continuous conversion.
- Operating voltage: support 2.0V≤V_{DD}≤5.5V operating voltage range.
- It can detect the built-in reference voltage (1.45V) and temperature sensors.

The ADC can set various A/D conversion modes by combining the modes described below.

Trigger mode	Software trigger	Start the conversion by operating the software.
	Hardware-trigger no-wait mode	The conversion is started by detecting a hardware trigger.
	Hardware trigger wait mode	In the conversion standby state when the power is cut off, the power is turned on by detecting the hardware trigger, and the conversion starts automatically after the A/D power stabilization waiting time.
Channel select mode	Select mode	Select 1 channel of analog input for A/D conversion.
	Scan mode	Four consecutive channels can be selected as analog inputs for sequential A/D conversion. Four consecutive channels from ANI0 to ANI15 can be selected as analog inputs.
Conversion mode	Single conversion mode	Perform an A/D conversion for the selected channel.
	Continuous conversion mode	Perform continuous A/D conversions for the selected channel until stopped by the software.
Sample time/ conversion time	Number of sample clocks/ conversion clocks	The sampling time can be set by register, the default value of sampling clock number is 13.5 clk, and the minimum value of conversion clock number is 31.5 clk.

6.25 Digital-to-analog converter (DAC)

This product has a built-in 2-channel 8-bit resolution analog-to-digital converter (DAC) that converts digital inputs to analog signals. It has the following features:

- 8-bit resolution D/A converter
- Support two independent analog channel outputs
- R-2R ladder network
- Built-in real-time output

6.26 Comparator (CMP)

This product has built-in two-channel comparators CMP0 and CMP1 with the following features:

- The CMP1 external input and reference multichannel can be selected.
- The external reference input and internal reference voltage can be selected for the reference voltage.
- The cancellation width of the noise cancellation digital filter can be selected.
- Can detect the active edge of the comparator output and generate an interrupt signal.
- Can detect the active edge of the comparator output and output the event signal to the linkage controller.

6.27 Programmable gain amplifier (PGA)

This product has two built-in programmable gain amplifiers (PGA0 and PGA1) with the following functions:

- There are 7 options for amplification gain per PGA: 4x, 8x, 10x, 12x, 14x, 16x, 32x.
- An external pin can be selected as ground for the negative feedback resistor of the PGA (which can be used in differential mode).
- The output of PGA0 can be selected as an analog input for the A/D converter or an analog input at the positive side of Comparator 0 (CMP0).
- The output of PGA1 can be selected as an analog input for the A/D converter

6.28 Two-wire serial debug port (SW-DP)

The ARM's SW-DP interface allows connection to the microcontroller via a serial line debugging tool.

6.29 Safety function

6.29.1 Flash CRC function (high-speed CRC, universal CRC)

Data errors in flash memory are detected by CRC operations.

The following two CRCs can be used for different applications and conditions of use.

- High-speed CRC: In the initialization program, it can stop the CPU and check the whole code flash area at high speed.
- Universal CRC: Can be used for multi-purpose checking during CPU operation, not limited to the code flash area.

6.29.2 RAM parity error detection function

Detect parity error when reading RAM data.

6.29.3 SFR guard function

Prevent rewriting of important SFRs (Special Function Registers) due to loss of CPU control.

6.29.4 Illegal memory access detection function

Detect illegal access to an illegal memory area (an area with no memory or an area with restricted access).

6.29.5 Frequency detection function

Able to use the Timer4 unit to self-test the CPU or peripheral hardware clock frequency.

6.29.6 A/D test function

The A/D converter is self-tested by A/D converting the positive (+) reference voltage, the negative (-) reference voltage, the analog input channel (ANI), the temperature sensor output voltage, and the internal reference voltage.

6.29.7 Digital output signal level detection function for input/output ports

When the input/output port is in output mode, the output level of the pin can be read.

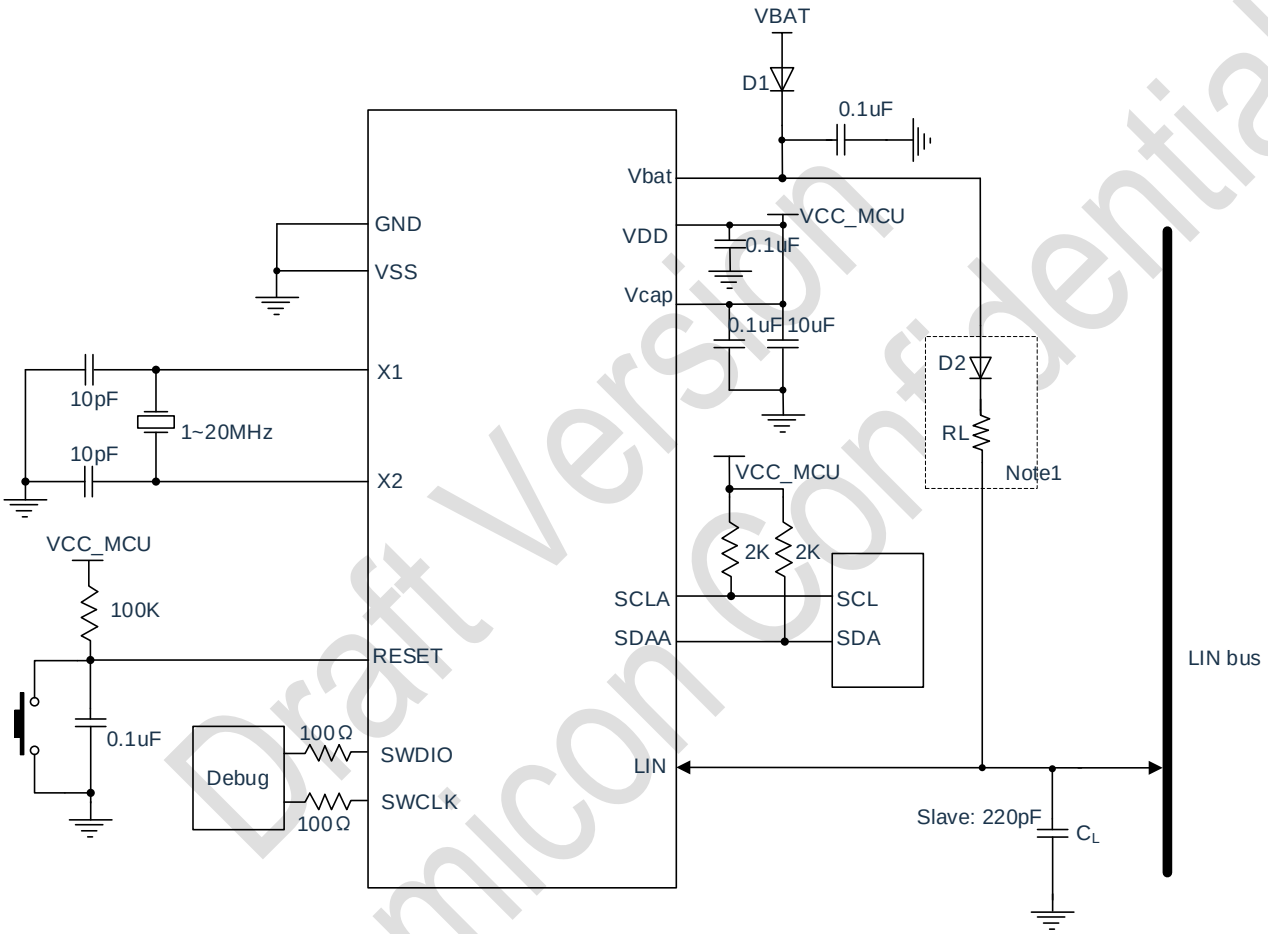
6.30 Key function

A key interrupt (INTKR) can be generated by inputting the falling edge of the key interrupt input pins (KR0~KR7).

7 Electrical Characteristics

7.1 Typical application peripheral circuits

The reference diagram for the connection of peripheral circuits for typical MCU applications is as follows:



Note 1: Connect D2, RL only when used as a master node;

Note 2: For the master node, a 660Ω/6.8nF RL/CL combination is recommended to obtain a slower slope of the bus waveform.

7.2 Absolute maximum voltage ratings

(T_A= -40~125°C)

Item	Symbol	Condition	Rating	Unit
Battery voltage	Vbat	-	-0.3~40	
MCU voltage	VDD	-	-0.5~6.5	V
Input voltage	V_{I1}	P00~P01, P10~P17, P31, P40~P41, P51, P72~P75, P120, P136, P140, P146, P147	-0.3~ VDD +0.3Note1	V
	V_{I2}	P60~P63(N-channel open-drain)	-0.3~6.5	V
	V_{I3}	P20~P27, P121~P124, P137, EXCLK, EXCLKS, RESETB	-0.3~ VDD +0.3Note1	V
Output voltage	V_{O1}	P00~P01, P10~P17, P31, P40~P41, P51, P60~P63, P72~P75, P120, P130, P136, P140, P146, P147	-0.3~ VDD +0.3Note1	V
	V_{O2}	P20~P27, P137	-0.3~ VDD +0.3Note1	V
Analog input voltage	V_{AI1}	ANI8~ANI12	-0.3~ VDD +0.3 and -0.3~AV_{REF}(+)+0.3Note1,2	V
	V_{AI2}	ANI0~ANI7	-0.3~ VDD +0.3 and -0.3~AV_{REF}(+)+0.3Note1,2	V

Note 1: Not more than 6.5V.

Note 2: The pin of the A/D conversion object cannot exceed AV_{REF} (+)+0.3.

Caution: Even if one item in each item instantly exceeds the absolute maximum rating, it may reduce the quality of the product. The absolute maximum rating is the rating that may cause physical damage to the product, and the product must be used in a state that do not exceed the ratings.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. AV_{REF}(+): The positive (+) reference voltage of the A/ D converter
3. Use V_{SS} as the reference voltage.
4. Low temperature specification is guaranteed by the design, and is not tested in mass production.

7.3 Absolute maximum current ratings

(T_A= -40~125°C)

Item	Symbol	Condition		Rating	Unit
Output current, high	I_{OH1}	Per pin	P00~P01, P10~P17, P31, P40~P41, P51, P72~P75, P120, P130, P136, P137, P140, P146, P147	-40	mA
		Pin total -170mA	P00~P01, P40~P41, P120, P130, P136, P137, P140, P141	-70	mA
			P10~P17, P31, P51, P72~P75, P146, P147	-100	mA
	I_{OH2}	Per pin	P20~P27	-3	mA
		Pin total		-15	mA
Output current, low	I_{OL1}	Per pin	P00~P01, P10~P17, P31, P40~P41, P51, P60~P63, P72~P75, P120, P130, P136, P137, P140, P146, P147	40	mA
		Pin total 170mA	P00~P01, P40~P41, P120, P130, P136, P137, P140	100	mA
			P10~P17, P31, P51, P72~P75, P146, P147	120	mA
	I_{OL2}	Per pin	P20~P27	15	mA
		Pin total		45	mA
Input current, negative	I_{INJL}	Per pin	Input pin continuous DC negative current	-3	mA
		Pin total		-15	mA
Input current, positive	I_{INJH}	Per pin	Input pin continuous DC positive current	3	mA
		Pin total		15	mA
Operating ambient temperature	T_A	Usually runtime		-40~125	°C
		When programming the flash memory			
Storage temperature	T_{stg}	-		-65~150	°C

Caution: Even if one item in each item instantly exceeds the absolute maximum rating, it may reduce the quality of the product. The absolute maximum rating is the rating that may cause physical damage to the product, and the product must be used in a state that do not exceed the ratings.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

7.4 Oscillation circuit characteristics

7.4.1 X1 and XT1 characteristics

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=0V)

Item	Resonator	Condition	Min.	Typ.	Max.	Unit
X1 clock oscillation frequency (F_X)	Ceramic/crystal resonator	-	1.0	-	20.0	MHz
X1 clock oscillation stabilization time	Ceramic/crystal resonator	20MHz, C=10pF	-	15	-	ms
X1 clock oscillation feedback resistor	Ceramic/crystal resonator	-	0.6	-	1.8	MΩ
XT1 clock oscillation frequency (F_{XT})	Crystal resonator	-	32	32.768	35	KHz
XT1 clock oscillation stabilization time	Crystal resonator	32.768KHz, C=20pF	-	2	-	s

Remark:

1. It only indicates the frequency tolerance range of the oscillation circuit, and the instruction execution time should be referred to the AC characteristics.
2. Please ask the resonator manufacturer to evaluate the circuit after installation, and use it after confirming the oscillation characteristics.
3. Low temperature specification is guaranteed by the design, and is not tested in mass production.

7.4.2 Internal oscillator characteristics

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=0V)

Resonator	Condition	Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency (F_{IH}) Note1,2	-	1.0	-	64.0	MHz
High-speed on-chip oscillator stabilization time (T_{SU})	-	-	12	-	us
Clock frequency accuracy of high-speed on-chip oscillator	T_A= 10~70℃	-1.0	-	+1.0	%
	T_A= 0~105℃	-1.5	-	+1.5	%
	T_A= -10~125℃	-2.0	-	+2.0	%
	T_A= -40~125℃	-4.0	-	+4.0	%
Low-speed on-chip oscillator clock frequency (F_{IL})	-	10	15	22	KHz

Note 1: Select the frequency of the high-speed on-chip oscillator via the option byte.

Note 2: It only indicates the characteristics of the oscillation circuit, so please refer to the AC characteristics for the instruction execution time.

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

7.5 DC characteristics

7.5.1 Pin characteristics

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output current, high[Note1]	I_{OH1}	P00~P01, P10~P17, P31, P40~P41, P51, P72~P75, P120, P130, P136, P137, P140, P146, P147 Per pin	2.0V≤VDD≤5.5V -40~85℃	-	-	-12.0[Note2]	mA
			2.0V≤VDD≤5.5V 85~125℃	-	-	-6.0[Note2]	
		P00~P01, P40~P41, P120, P130, P136, P137, P140, Total (when duty cycle≤ 70%[Note3])	4.0V≤VDD≤5.5V -40~85℃	-	-	-60.0	mA
			4.0V≤VDD≤5.5V 85~125℃	-	-	-30.0	
			2.4V≤VDD<4.0V	-	-	-12.0	mA
			2.0V≤VDD<2.4V	-	-	-6.0	mA
		P10~P17, P31, P51, P72~P75, P146, P147 Total (when duty cycle≤ 70%[Note3])	4.0V≤VDD≤5.5V -40~85℃	-	-	-80.0	mA
			4.0V≤VDD≤5.5V 85~125℃	-	-	-30.0	
			2.4V≤VDD<4.0V	-	-	-20.0	mA
			2.0V≤VDD<2.4V	-	-	-10.0	mA
		Total (when duty cycle≤ 70%[Note3])	4.0V≤VDD≤5.5V -40~85℃	-	-	-140.0	mA
			4.0V≤VDD≤5.5V 85~125℃	-	-	-60.0	
			2.4V≤VDD≤4.0V	-	-	-30.0	
			2.0V≤VDD≤2.4V	-	-	-15.0	
	I_{OH2}	P20~P27 Per pin	2.0V≤VDD≤5.5V	-	-	-2.5[Note2]	mA
		Total (when duty cycle≤ 70%[Note3])	2.0V≤VDD≤5.5V	-	-	-10	mA

Note 1: This is the value of current that guarantees the operation of the device even if current flows from the V_{DD} pins to the output pins.

Note 2: The total current value cannot be exceeded.

Note 3: This is the output current value for the “Duty cycle ≤ 70% condition”.

The following formula can be used to calculate the output current value when the duty cycle is changed to >70% (when the duty cycle is changed to n%).

Total pin output current=(I_{OH}×0.7)/(n×0.01)

<Calculation example> I_{OH} =–10.0mA, n =80%

Total pin output current = (–10.0×0.7)/(80×0.01) ≈ –8.7mA

The current at each pin does not vary by duty cycle and will not flow above the absolute maximum rating.

Caution: In N-channel open drain mode, P00, P01, P10, P11, P13~P15, P17, P51, P55, P74 do not output high level.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.

2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output current, low[Note1]	I_{OL1}	P00~P01, P10~P17, P31, P40~P41, P51, P60~P63, P72~P75, P120, P130, P136, P137, P140, P146, P147 Per pin	2.0V≤VDD≤5.5V -40~85℃	-	-	30[Note2]	mA
			2.0V≤VDD≤5.5V 85~125℃	-	-	15[Note2]	
		P00~P01, P40~P41, P120, P130, P136, P137, P140, Total (when duty cycle≤ 70%[Note3])	4.0V≤VDD≤5.5V -40~85℃	-	-	100	mA
			4.0V≤VDD≤5.5V 85~125℃	-	-	50	
			2.4V≤VDD<4.0V	-	-	30	mA
			2.0V≤VDD<2.4V	-	-	15	mA
		P10~P17, P31, P51, P60~P63, P72~P75, P146, P147 Total (when duty cycle≤ 70%[Note3])	4.0V≤VDD≤5.5V -40~85℃	-	-	120	mA
			4.0V≤VDD≤5.5V 85~125℃	-	-	60	
			2.4V≤VDD<4.0V	-	-	40	mA
			2.0V≤VDD<2.4V	-	-	20	mA
		Total (when duty cycle≤ 70%[Note3])	4.0V≤VDD≤5.5V -40~85℃	-	-	150	mA
			4.0V≤VDD≤5.5V 85~125℃	-	-	80	
			2.4V≤VDD≤4.0V	-	-	50	
			2.0V≤VDD≤2.4V	-	-	30	
	I_{OL2}	P20~P27 Per pin	2.0V≤VDD≤5.5V	-	-	6[Note2]	mA
		Total (when duty cycle≤ 70%[Note3])	2.0V≤VDD≤5.5V	-	-	20	mA

Note1: This is the value of current that guarantees the operation of the device even if current flows from the output pins to the GND or V_{SS} pins.

Note2: The total current value cannot be exceeded.

Note3: This is the output current value for the “Duty cycle ≤ 70% condition”.

The following formula can be used to calculate the output current value when the duty cycle is changed to >70% (n% duty cycle).

Total output current = (I_{OL}×0.7)/(n×0.01)

<Calculation example> I_{OL}= 10.0mA, n = 80%

Total output current = (10.0×0.7)/(80×0.01) ≈ 8.7mA

The current at each pin does not vary by duty cycle and will not flow above the absolute maximum rating.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Battery voltage	Vbat	-		5.5		28	V
LDO output voltage	Vcap	-		4.9		5.1	V
MCU input voltage	VDD	-		2.0	-	5.5	V
Power ground input voltage	V_{SS} GND	-		-0.3	-	-	V
Input voltage, high	V_{IH1}	P00~P01, P10~P17, P31, P40~P42, P51, P72~P75, P120, P136, P140, P146, P147	Schmitt input	0.8VDD	-	VDD	V
	V_{IH2}	P01, P10, P14~P17, P30	TTL input 4.0V≤VDD≤5.5V	2.2	-	VDD	V
			TTL input 3.3V≤VDD＜4.0V	2.0	-	VDD	V
			TTL input 2.0V≤VDD＜3.3V	1.5	-	VDD	V
	V_{IH3}	P20~P27, P137		0.7VDD	-	VDD	V
	V_{IH4}	P60~P63		0.7VDD	-	6.0	V
	V_{IH5}	P121~P124, EXCLK, EXCLKS, RESETB		0.8VDD	-	VDD	V
Input voltage, low	V_{IL1}	P00~P01, P10~P17, P31, P40~P41, P51, P72~P75, P120, P136, P140, P146, P147	Schmitt input	0	-	0.2VDD	V
	V_{IL2}	P01, P10, P14~P17	TTL input 4.0V≤VDD≤5.5V	0	-	0.8	V
			TTL input 3.3V≤VDD＜4.0V	0	-	0.5	V
			TTL input 2.0V≤VDD＜3.3V	0	-	0.32	V
	V_{IL3}	P20~P27, P137		0	-	0.3VDD	V
	V_{IL4}	P60~P63		0	-	0.3VDD	V
	V_{IL5}	P121~P124, EXCLK, EXCLKS, RESETB		0	-	0.2VDD	V

Caution: Even in N-channel open drain mode, the maximum V_{IH} value for P00, P01, P10, P11, P13~P15, P17, P51, P55 and P74 is V_{DD}.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40 ~125°C, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output voltage, high	V_{OH1}	P00~P01, P10~P17, P31, P40~P41, P51, P72~P75, P120, P130, P136, P137, P140, P146, P147	4.0V≤VDD≤5.5V, I_{OH1}= -12.0mA	VDD-1.5	-	-	V
			4.0V≤VDD≤5.5V, I_{OH1}= -6.0mA	VDD-0.7	-	-	V
			2.4V≤VDD≤5.5V, I_{OH1}= -3.0mA	VDD-0.6	-	-	V
			2.0V≤VDD≤5.5V, I_{OH1}= -2mA	VDD-0.5	-	-	V
	V_{OH2}	P20~P27	4.0V≤VDD≤5.5V, I_{OH2}= -2.5mA	VDD-1.5	-	-	V
			4.0V≤VDD≤5.5V, I_{OH2}= -1.5mA	VDD-0.7	-	-	V
			2.4V≤VDD≤5.5V, I_{OH2}= -0.5mA	VDD-0.6	-	-	V
			2.0V≤VDD≤5.5V, I_{OH2}= -0.4mA	VDD-0.5	-	-	V
Output voltage, low	V_{OL1}	P00~P01, P10~P17, P31, P40~P41, P51, P60~P63, P72~P75, P120, P130, P136, P137, P140, P146, P147	4.0V≤VDD≤5.5V, I_{OL1}=30.0mA	-	-	1.2	V
			4.0V≤VDD≤5.5V, I_{OL1}=15.0mA	-	-	0.7	V
			2.4V≤VDD≤5.5V, I_{OL1}=6.0mA	-	-	0.4	V
			2.0V≤VDD≤5.5V, I_{OL1}=4.0mA	-	-	0.4	V
	V_{OL2}	P20~P27	4.0V≤VDD≤5.5V, I_{OL2}=6.0mA	-	-	1.2	V
			4.0V≤VDD≤5.5V, I_{OL2}=4.0mA	-	-	0.7	V
			2.4V≤VDD≤5.5V, I_{OL2}=1.5mA	-	-	0.4	V
			2.0V≤VDD≤5.5V, I_{OL2}=1.0mA	-	-	0.4	V

Caution: In N-channel open drain mode, P00, P02~P04, P10, P11, P13~P15, P17, P30, P50, P51, P55, P71, P74 do not output high level.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input leakage current, high	I_{LIH1}	P00~P01, P10~P17, P31, P40~P41, P51, P72~P75, P120, P136, P140, P146, P147	V_I= VDD	-	-	1	uA
	I_{LIH2}	P20~P27, P137, RESETB	V_I= VDD	-	-	1	uA
	I_{LIH3}	P121~P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I= VDD, when the input port and external clock are inputting	-	-	1	uA
			V_I= VDD, when connecting the resonator	-	-	10	uA
Input leakage current, low	I_{LIL1}	P00~P01, P10~P17, P31, P40~P41, P51, P72~P75, P120, P136, P140, P146, P147	V_I=V_{SS}	-	-	-1	uA
	I_{LIL2}	P20~P27, P137, RESETB	V_I=V_{SS}	-	-	-1	uA
	I_{LIL3}	P121~P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I=V_{SS}, when the input port and external clock are inputting	-	-	-1	uA
			V_I=V_{SS}, when connecting the resonator	-	-	-10	uA
Internal pull-up resistance	R_U	P00~P01, P10~P17, P31, P40~P41, P51, P72~P75, P120, P136, P137, P140, P146, P147	V_I=V_{SS}, when inputting a port	10	30	100	KΩ

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

7.5.2 Power supply current characteristics

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition				Min.	Typ.	Max.	Unit
MCU current Note 1	I_{DD1}	Run mode	High-speed on-chip oscillator	F_{HOCO}=64MHz, F_{IH}=32MHz Note3		-	4.6	10.5	mA
				F_{HOCO}=48MHz, F_{IH}=48MHz Note3		-	4.9	11.5	
				F_{HOCO}=32MHz, F_{IH}=32MHz Note3		-	4.4	9.0	
			High-speed main system clock	F_{MX}=20MHz Note2	Input square wave	-	2.3	5.4	mA
					Connect the crystal oscillator	-	2.3	5.4	
			Subsystem clock operation	F_{SUB}=32.768KHz Note4	Input square wave	-	70	120	uA
					Connect the crystal oscillator	-	70	120	
	I_{DD2}	Sleep mode	High-speed on-chip oscillator	F_{HOCO}=64MHz, F_{IH} =32MHz Note3		-	1.2	5.8	mA
				F_{HOCO}=48MHz, F_{IH} =48MHz Note3		-	1.2	6.5	
				F_{HOCO}=32MHz, F_{IH} =32MHz Note3		-	1.2	4.5	
			High-speed main system clock	F_{MX} =20MHz Note2	Input square wave	-	0.7	2.0	mA
					Connect the crystal oscillator	-	0.7	2.0	
			Subsystem clock operation	F_{SUB} =32.768KHz Note5	Input square wave	-	0.7	40	uA
					Connect the crystal oscillator	-	0.7	40	
	I_{DD3} Note6	Deep sleep mode Note7	T_A= -40℃~25℃ VDD=5.0V			-	0.45	1.1	uA
			T_A= -40℃~85℃ VDD=5.0V			-	0.45	8.0	
			T_A= -40℃~105℃ VDD=5.0V			-	0.45	12.5	
			T_A= -40℃~125℃ VDD=5.0V			-	0.45	35	

Note1: This is the total current through V_{DD}, including input leakage current fixed to V_{DD} or V_{SS} on the input pin. Typical alue: CPU is multiplied. Algorithm instruction execution (I_{DD1}) and does not include external operating current. Maximum Value: The CPU is in multiply instruction execution (I_{DD1}) and contains external operating current, but does not include current to the A/ D converter, LVD circuitry, I/O ports, and internal pull-up or pull-down resistors, nor does it include the current when overwriting the data flash memory.

Note2: This is when the high-speed internal oscillator and the subsystem clock stop oscillating.

Note3: This is when the high-speed primary and secondary system clocks stop oscillating.

Note4: This is when the high-speed internal oscillator and the high-speed main system clock stop oscillating.

Note5: This is when the high-speed internal oscillator and the high-speed main system clock stop oscillating. Contains current to the RTC, but does not include current to 15-bit interval timers and watchdog timers.

Note6: Current to RTC, 15-bit interval timers, and watchdog timers is not included.

Note7: For the current value when the secondary system clock is running in deep sleep mode, refer to the current value when the secondary system clock is running in sleep mode.

Remark:

1. F_{HOCO}: The clock frequency of the high-speed internal oscillator, F_{IH}: The system clock frequency provided by the high-speed internal oscillator.

2. F_{SUB}: External subsystem clock frequency (XT1/ XT2 clock oscillation frequency).
3. F_{MX}: External main system clock frequency (X1/ X2 clock oscillation frequency).
4. TYP. The temperature condition of the value is T_A=25℃.
5. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~125℃, Vbat = 12V, V_{SS}=GND=0V)

Item	Symbol	Condition				Min.	Typ.	Max.	Unit
Vbat pin current	I_{bat1}	Run mode Note1	High-speed on-chip oscillator	F_{HOCO}=64MHz, F_{IH}=32MHz		-	TBD	TBD	mA
				F_{HOCO}=48MHz, F_{IH}=48MHz		-	TBD	TBD	
				F_{HOCO}=32MHz, F_{IH}=32MHz		-	TBD	TBD	
			High-speed main system clock	F_{MX}=20MHz	Input square wave	-	TBD	TBD	mA
					Connect the crystal oscillator	-	TBD	TBD	
			Subsystem clock operation	F_{SUB}=32.768KHz	Input square wave	-	TBD	TBD	mA
					Connect the crystal oscillator	-	TBD	TBD	
	I_{bat2}	Sleep mode Note2	High-speed on-chip oscillator	F_{HOCO}=64MHz, F_{IH} =32MHz		-	TBD	TBD	mA
				F_{HOCO}=48MHz, F_{IH} =48MHz		-	TBD	TBD	
				F_{HOCO}=32MHz, F_{IH} =32MHz		-	TBD	TBD	
			High-speed main system clock	F_{MX} =20MHz	Input square wave	-	TBD	TBD	mA
					Connect the crystal oscillator	-	TBD	TBD	
			Subsystem clock operation	F_{SUB} =32.768KHz	Input square wave	-	TBD	TBD	uA
					Connect the crystal oscillator	-	TBD	TBD	
	I_{bat3}	Deep sleep mode Note3	T_A= -40℃~25℃			-	TBD	TBD	uA
			T_A= -40℃~85℃			-	TBD	TBD	
			T_A= -40℃~105℃			-	TBD	TBD	
			T_A= -40℃~125℃			-	TBD	TBD	
	I_{bat4}	Stop mode Note4	T_A= -40℃~125℃			-	TBD	TBD	uA

Note1: Run mode, MCU is in running state, LIN transceiver operates normally, LDO outputs 5V, and the maximum driving current is 70mA.

Note2: Sleep mode, CPU clock is stopped, peripherals can operate as set, LIN transceiver is in standby state, LDO continues to output 5V, with a driving capability of 70mA, and the system can be woken up by an external interrupt.

Note3: Deep sleep mode, high-speed system clock and entire system are stopped, LIN transceiver is in standby state, LDO continues to output 5V, with a driving current of 70mA, and the system can be woken up by an external interrupt.

Note4: Stop mode, LDO stops outputting 5V, MCU is powered off, LIN transceiver is in sleep state, and the system can be remotely woken up via the LIN bus.

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Low speed on-chip oscillator operating current	I_{FIL} Note1	-		-	0.2	-	uA
RTC operating current	I_{RTC} Note1,2,3	-		-	0.04	-	uA
15-bit interval timer operating current	I_{IT} Note1,2,4	-		-	0.02	-	uA
Watchdog timer operating current	I_{WDT} Note1,2,5	F_{IL}=15KHz		-	0.22	-	uA
A/D converter operating current	I_{ADC} Note1,6	ADC HS mode@64MHz		-	2.2	-	mA
		ADC HS mode @4MHz		-	1.3	-	mA
		ADC LC mode @24MHz		-	1.1	-	mA
		ADC LC mode @4MHz		-	0.8	-	mA
D/A converter operating current	I_{DAC} Note1,8	Per channel		-	1.4	-	mA
PGA operating current		Per channel		-	480	700	uA
Comparator operating current	I_{CMP} Note1,9	Per channel	No internal reference voltage is used	-	60	100	uA
			An internal reference voltage is used	-	80	140	uA
LVD operating current	I_{LVD} Note1,7	-		-	0.08		uA

Note1: This is the current flowing through V_{DD}.

Note2: This is when the high-speed internal oscillator and the high-speed system clock stop oscillating.

Note3: This is the current that flows only to the real-time clock (RTC) (excluding the operating current of the low-speed internal oscillator and the XT1 oscillation circuit). In the case of a real-time clock operating in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{RTC} value. In addition, I_{FIL} must be added when selecting a low-speed internal oscillator. I_{DD2} when the secondary system clock is running contains the operating current of the real-time clock.

Note4: This is the current that flows only to the 15-bit interval timer (excluding the operating current of the low-speed internal oscillator and XT1 oscillation circuit). In the case of 15-bit interval timer operation in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{IT} value. In addition, I_{FIL} must be added when selecting a low-speed internal oscillator.

Note5: This is the current that flows only to the watchdog timer (including the operating current of the low-speed internal oscillator). In the case of watchdog timer operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus I_{WDT}.

Note6: This is the current that only flows to the A/ D converter. In the case of A/ D converter operation in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{ADC} value.

Note7: This is the current that only flows to the LVD circuit. In the case of LVD circuit operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the value of I_{LVD}.

Note8: This is the current that only flows to the D/ A converter. In the case of D/ A converter operation in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{DAC} value.

Note9: This is the current that only flows to the comparator circuit. In the case of comparator circuit operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the I_{CMP} value.

Remark:

1. F_{IL}: The clock frequency of the low-speed internal oscillator
2. TYP. The temperature condition of the value is T_A=25℃.
3. Low temperature specification is guaranteed by the design, and is not tested in mass production.

7.6 AC characteristics

(T_A= -40~125°C, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (F_{MAIN}) is running	2.0V≤VDD≤5.5V	0.02084	-	1	us
		Subsystem clock (F_{SUB}) is running	2.0V≤VDD≤5.5V	28.5	30.5	31.3	us
External system clock frequency	F_{EX}	2.0V≤VDD≤5.5V		1.0	-	20.0	MHz
	F_{EXS}	2.0V≤VDD≤5.5V		32.0	-	35.0	KHz
High/low widths of external system clock inputs	T_{EXH}, T_{EXL}	2.0V≤VDD≤5.5V		24	-	-	ns
	T_{EXHS}, T_{EXLS}	2.0V≤VDD≤5.5V		13.7	-	-	us
TI00~TI03, input high/low level width	T_{TIH}, T_{TIL}	2.0V≤VDD≤5.5V		1/F_{MCK} +10	-	-	ns
Input period of TimerA	T_C	TAIO	2.4V≤VDD≤5.5V	100	-	-	ns
			2.0V≤VDD<2.4V	300	-	-	ns
High and low width of TimerA input	T_{TAIH}, T_{TAIL}	TAIO	2.4V≤VDD≤5.5V	40	-	-	ns
			2.0V≤VDD<2.4V	120	-	-	ns

Remark:

1. F_{MCK}: The operating clock frequency of the Timer4 unit
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High and low width of timer M input	T_{TMIH}, T_{TMIL}	TMIOA0, TMIOA1, TMIOB0, TMIOB1, TMIOC0, TMIOC1, TMIOD0, TMIOD1		3/F_{CLK}	-	-	ns
Low width of Timer M forced cutoff signal input	T_{TMSIL}	P136/INTP0	2MHz＜F_{CLK}≤48MHz	1	-	-	us
			F_{CLK} ≤2MHz	1/F_{CLK} +1	-	-	us
High/low width of timer B input	T_{TBIH}, T_{TBIL}	TBIOA, TBIOB		2.5/F_{CLK}	-	-	ns
Output frequency of TO00 ~ TO03, TAIO0, TAO0, TMIOA0, TMIOA1, TMIOB0, TMIOB1, TMIOC0, TMIOC1, TMIOD0, TMIOD1, TBIOA, TBIOB	F_{TO}	4.0V≤VDD≤5.5V		-	-	16	MHz
		2.4V≤VDD＜4.0V		-	-	8	MHz
		2.0V≤VDD＜2.4V		-	-	4	MHz
Output frequency of CLKBUZ0, CLKBUZ1	F_{PCL}	4.0V≤VDD≤5.5V		-	-	16	MHz
		2.4V≤VDD＜4.0V		-	-	8	MHz
		2.0V≤VDD＜2.4V		-	-	4	MHz
High/low width of interrupt input	T_{INTH}, T_{INTL}	INTP0~INTP11	2.0V≤VDD≤5.5V	1	-	-	us
High/low level width of key interrupt input	T_{KR}	KR0~KR7	2.0V≤VDD≤5.5V	250	-	-	ns
Low-level width of RESETB	T_{RSL}	-		10	-	-	us

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

7.7 Peripheral function characteristics

7.7.1 Universal interface unit

(1) UART mode

(T_A= -40~85℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Condition		Specification value		Unit
			Min.	Max.	
Transfer rate	2.0V ≤VDD ≤ 5.5V	-	-	F_{MCK} /6	bps
		Theoretical value of the maximum transfer rate F_{MCK} = F_{CLK}	-	8	Mbps

(T_A=+85~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Condition		Specification value		Unit
			Min.	Max.	
Transfer rate	2.0V ≤VDD ≤ 5.5V	-	-	F_{MCK} /12	bps
		Theoretical value of the maximum transfer rate F_{MCK} = F_{CLK}	-	4	Mbps

Remark: It is guaranteed by the design, and is not tested in mass production.

(2) 3-wire SPI mode (master mode, internal clock output)

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		-40~85℃		85~125℃		Unit
				Min.	Max.	Min.	Max.	
SCLKp cycle time	T_{KCY1}	T_{KCY1} ≥ 2/ F_{CLK}	4.0V ≤VDD ≤ 5.5V	41.67	-	83.33	-	ns
			2.7V ≤VDD ≤ 5.5V	83.33	-	166.67	-	ns
			2.4V ≤VDD ≤ 5.5V	125	-	250	-	ns
			2.0V ≤VDD ≤ 5.5V	250	-	500	-	ns
SCLKp high/low level width	T_{KH1}, T_{KL1}	4.0V ≤VDD ≤ 5.5V		T_{KCY1}/2-7	-	T_{KCY1}/2-14	-	ns
		2.7V ≤VDD ≤ 5.5V		T_{KCY1}/2-10	-	T_{KCY1}/2-20	-	ns
		2.4V ≤VDD ≤ 5.5V		T_{KCY1}/2-18	-	T_{KCY1}/2-36	-	ns
		2.0V ≤VDD ≤ 5.5V		T_{KCY1}/2-38	-	T_{KCY1}/2-76	-	ns
SDIp set-up time (for SCLKp↑)	T_{SIK1}	4.0V ≤VDD ≤ 5.5V		23	-	46	-	ns
		2.7V ≤VDD ≤ 5.5V		33	-	66	-	ns
		2.4V ≤VDD ≤ 5.5V		44	-	88	-	ns
		2.0V ≤VDD ≤ 5.5V		75	-	113	-	ns
SDIp hold time (for SCLKp↑)	T_{KSI1}	2.0V ≤VDD ≤ 5.5V		10	-	20	-	ns
Delay time from SCLKp↓→SDOp	T_{KSO1}	2.0V ≤VDD ≤ 5.5V C=20pF[Note1]		-	10	-	20	ns

Note1: C is the load capacitance of the SCLKp, SDOp output lines.

Caution: Through the Port Input Mode Register and Port Output Mode Register, the SDIp pin is selected as the normal input buffer and the SDOp pin and SCLKp pin are selected as the normal output mode.

Remark: It is guaranteed by the design, and is not tested in mass production.

(3) 3-wire SPI mode (slave mode, external clock input)

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		-40~85℃		85~125℃		Unit
				Min.	Max.	Min.	Max.	
SCLKp cycle time	T_{KCY2}	4.0V ≤VDD ≤ 5.5V	20MHz＜F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK} ≤20MHz	6/F_{MCK}	-	12/F_{MCK}	-	ns
		2.7V ≤VDD ≤ 5.5V	16MHz ＜ F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK} ≤16MHz	6/F_{MCK}	-	12/F_{MCK}	-	ns
		2.4V ≤VDD ≤ 5.5V		6/F_{MCK} and ≥500	-	12/F_{MCK} and≥1000	-	ns
		2.0V ≤VDD ≤ 5.5V		6/F_{MCK} and≥750	-	12/F_{MCK} and≥1500	-	ns
SCLKp high/low level width	T_{KH2} T_{KL2}	4.0V ≤VDD ≤ 5.5V		T_{KCY1}/2-7	-	T_{KCY1}/2-14	-	ns
		2.7V ≤VDD ≤ 5.5V		T_{KCY1}/2-8	-	T_{KCY1}/2-16	-	ns
		2.0V ≤VDD ≤ 5.5V		T_{KCY1}/2-18	-	T_{KCY1}/2-36	-	ns
SDIp set-up time (for SCLKp↑)	T_{SIK2}	2.7V ≤VDD ≤ 5.5V		1/F_{MCK}+20	-	1/F_{MCK} +40	-	ns
		2.0V ≤VDD ≤ 5.5V		1/F_{MCK}+30	-	1/F_{MCK} +60	-	ns
SDIp hold time (for SCLKp↑)	T_{KSI2}	2.0V ≤VDD ≤ 5.5V		1/F_{MCK}+31	-	1/F_{MCK} +62	-	ns
Delay time from SCLKp↓ →SDOp	T_{KSO2}	2.7V ≤VDD ≤ 5.5V C=30pF[Note1]		-	2/F_{MCK}+44	-	2/F_{MCK}+66	ns
		2.4V ≤VDD ≤ 5.5V C=30pF[Note1]		-	2/F_{MCK}+75	-	2/F_{MCK}+113	ns
		2.0V ≤VDD ≤ 5.5V C=30pF[Note1]		-	2/F_{MCK}+100	-	2/F_{MCK}+150	ns

Note1: C is the load capacitance of the SCLKp, SDOp output lines.

Caution: Through the Port Input Mode Register and Port Output Mode Register, the SDIp and SCLKp pins are selected as the normal input buffers and the SDOp pin is selected as the normal output mode.

Remark: It is guaranteed by the design, and is not tested in mass production.

(4) 4-wire SPI mode (slave mode, external clock input)

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		-40~85℃		85~125℃		Unit
				Min.	Max.	Min.	Max.	
SSI00 set-up time	T_{SSIK}	DAPmn=0	2.7V ≤VDD ≤ 5.5V	120	-	240	-	ns
			2.0V ≤VDD ≤ 5.5V	200	-	400	-	ns
		DAPmn=1	2.7V ≤VDD ≤ 5.5V	1/F_{MCK}+120	-	1/F_{MCK}+240	-	ns
			2.0V ≤VDD ≤ 5.5V	1/F_{MCK}+200	-	1/F_{MCK}+400	-	ns
SSI00 hold time	T_{KSSI}	DAPmn=0	2.7V ≤VDD ≤ 5.5V	1/F_{MCK}+120	-	1/F_{MCK}+240	-	ns
			2.0V ≤VDD ≤ 5.5V	1/F_{MCK}+200	-	1/F_{MCK}+400	-	ns
		DAPmn=1	2.7V ≤VDD ≤ 5.5V	120	-	240	-	ns
			2.0V ≤VDD ≤ 5.5V	200	-	400	-	ns

Caution: Select the SDIp and SCLKp pins as the normal input buffers and the SDOp pin as the normal output mode via the Port Input Mode Register and Port Output Mode Register.

Remark: It is guaranteed by the design, and is not tested in mass production.

(5) Simplified IIC mode

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition	-40~85℃		85~125℃		Unit
			Min.	Max.	Min.	Max.	
SCLr clock frequency	F_{SCL}	2.7V ≤VDD ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	-	1000[Note1]	-	400[Note1]	KHz
		2.0V ≤VDD ≤ 5.5V C_b = 100 pF, R_b = 3KΩ	-	400[Note1]	-	100[Note1]	KHz
		2.0V ≤VDD ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	-	300[Note1]	-	75[Note1]	KHz
Hold time when SCLr is low	T_{LOW}	2.7V ≤VDD ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	475	-	1200	-	ns
		2.0V ≤VDD ≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	1150	-	4600	-	ns
		2.0V ≤VDD ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1550	-	6500	-	ns
Hold time when SCLr is high	T_{HIGH}	2.7V ≤VDD ≤ 5.5V C_b = 50 pF, R_b = 2.7KΩ	475	-	1200	-	ns
		2.0V ≤VDD ≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	1150	-	4600	-	ns
		2.0V ≤VDD ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1550	-	6500	-	ns
Data setup time (reception)	$T_{SU: DAT}$	2.7V ≤VDD ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	1/F_{MCK}+85[Note2]	-	1/F_{MCK}+220[Note2]	-	ns
		2.0V ≤VDD ≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	1/F_{MCK}+145[Note2]	-	1/F_{MCK}+580[Note2]	-	ns
		2.0V ≤VDD ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1/F_{MCK}+230[Note2]	-	1/F_{MCK}+1200[Note2]	-	ns
Data hold time (transmission)	$T_{HD: DAT}$	2.7V ≤VDD ≤ 5.5V C_b = 50 pF, R_b = 2.7KΩ	-	305	-	770	ns
		2.0V ≤VDD ≤ 5.5V C_b = 100 pF, R_b = 3KΩ	-	355	-	1420	ns
		2.0V ≤VDD ≤ 2.7V C_b = 100 pF, R_b = 5KΩ	-	405	-	2070	ns

Note1: The value must also be equal to or less than F_{MCK}/4

Note2: Set the F_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Remark: It is guaranteed by the design, and is not tested in mass production.

7.7.2 Serial interface IICA

1) I²C standard mode

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}= GND=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLA0 clock frequency	F_{SCL}	Standard mode: F_{CLK}≥1MHz	-	100	KHz
Set-up time of the start condition	$T_{SU: STA}$	-	4.7	-	us
Hold time of the start condition Note1	$T_{HD: STA}$	-	4.0	-	us
Hold time when SCLA0 is low	T_{LOW}	-	4.7	-	us
Hold time when SCLA0 is high	T_{HIGH}	-	4.0	-	us
Data set-up time (reception)	$T_{SU: DAT}$	-	250	-	ns
Data hold time (transmission) Note2	$T_{HD: DAT}$	-	0	3.45	us
Set-up time of the stop condition	$T_{SU: STO}$	-	4.0	-	us
Bus idle time	T_{BUF}	-	4.7	-	us

Note1: Generate the first clock pulse after a start condition or a restart condition is generated.

Note2: The maximum value of $T_{HD: DAT}$ needs to be guaranteed during normal transfer and needs to be waited during ACK.

Caution: The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:

Standard mode: C_b=400pF, R_b=2.7KΩ

Remark: It is guaranteed by the design, and is not tested in mass production.

2) I²C fast mode

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLA0 clock frequency	F_{SCL}	Fast mode: F_{CLK}≥3.5MHz		400	KHz
Set-up time of the start condition	$T_{SU: STA}$	-	0.6	-	us
Hold time of the start condition Note1	$T_{HD: STA}$	-	0.6	-	us
Hold time when SCLA0 is low	T_{LOW}	-	1.3	-	us
Hold time when SCLA0 is high	T_{HIGH}	-	0.6	-	us
Data set-up time (reception)	$T_{SU: DAT}$	-	100	-	ns
Data hold time (transmission) Note2	$T_{HD: DAT}$	-	0	0.9	us
Set-up time of the stop condition	$T_{SU: STO}$	-	0.6	-	us
Bus idle time	T_{BUF}	-	1.3	-	us

Note1: Generate the first clock pulse after a start condition or a restart condition is generated.

Note2: The maximum (MAX.) value of $T_{HD: DAT}$ needs to be guaranteed during normal transfer and needs

to be waited during ACK.

Caution: The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:

Fast mode: C_b=320pF, R_b=1.1KΩ

Remark: It is guaranteed by the design, and is not tested in mass production.

3) I²C enhanced fast mode

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLA0 clock frequency	F_{SCL}	Enhanced fast mode: F_{CLK}≥10MHz	-	1000	KHz
Set-up time of the start condition	$T_{SU: STA}$	-	0.26	-	us
Hold time of the start condition Note1	$T_{HD: STA}$	-	0.26	-	us
Hold time when SCLA0 is low	T_{LOW}	-	0.5	-	us
Hold time when SCLA0 is high	T_{HIGH}	-	0.26	-	us
Data set-up time (reception)	$T_{SU: DAT}$	-	50	-	ns
Data hold time (transmission) Note2	$T_{HD: DAT}$	-	0	0.45	us
Set-up time of the stop condition	$T_{SU: STO}$	-	0.26	-	us
Bus idle time	T_{BUF}	-	0.5	-	us

Note1: Generate the first clock pulse after a start condition or restart condition is generated.

Note2: The maximum value of $T_{HD: DAT}$ needs to be guaranteed during normal transfer and needs to be waited during ACK.

Caution: The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:

Enhanced fast mode: C_b=120pF, R_b=1.1KΩ

Remark: It is guaranteed by the design, and is not tested in mass production.

7.8 Analog characteristics

7.8.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel \ Reference voltage	Reference voltage(+)=AV_{REFP} Reference voltage(–)=AV_{REFM}	Reference voltage(+)=V_{DD} Reference voltage (–)=V_{SS}
ANI0~ANI15	See 7.8.1(1)	See 7.8.1(2)
Internal reference voltage, temperature sensor output voltage		

(1) When selecting reference voltage (+)=AV_{REFP}/ANI0, reference voltage (-)=AV_{REFM}/ANI1
(T_A= -40~125℃, 2.0V≤AV_{REFP}≤VDD≤5.5V, V_{SS}=0V, reference voltage (+)=AV_{REFP},
reference voltage (-)= AV_{REFM} =0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	RES	-		-	12	-	bit
Combined error Note1	ET	12-bit resolution	2.0V ≤ AV_{REFP}≤ 5.5V	-	3	-	LSB
Zero scale error Note1	E_{ZS}	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Full scale error Note1	E_{FS}	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Integral linearity error Note1	EL	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-1	-	1	LSB
Differential linearity error Note1	ED	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-1.5	-	1.5	LSB
Conversion time Note3	T_{CONV}	12-bit resolution Conversion object: ANI2~ANI15	2.0V ≤VDD≤ 5.5V	45	-	-	1/F_{ADC}
		12-bit resolution Conversion object: internal reference voltage, temperature sensor output voltage, PGA output voltage	2.0V ≤VDD≤ 5.5V	72	-	-	1/F_{ADC}
External input resistance	R_{AIN}	R_{AIN} ＜(Ts /(F_{ADC} x C_{ADC} x ln(2^{12+2}))- R_{ADC})		-	10 Note4	-	KΩ
Sampling switch resistance	R_{ADC}	-		-	-	1.5	KΩ
Sample-and-hold capacitance	C_{ADC}	-		-	2	-	pF
Analog input voltage	V_{AIN}	ANI2~ANI15		0	-	AV_{REF}	V
		Internal reference voltage (2.0V≤VDD≤5.5V)		V_{BGR} Note2			V
		Temperature sensor output voltage (2.0V≤VDD≤5.5V)		V_{TMPS25} Note2			V

Note1: Quantization error (±1/2 LSB) is not included.

Note2: Please refer to “7. 8. 2 Characteristics of temperature sensor/internal reference voltage”.

Note3: F_{ADC} is the operation frequency of the AD, and the maximum operation frequency is 48MHz.

Note4: It is guaranteed by the design, and is not tested in mass production. The typical value is the default sampling period Ts=13.5, and the conversion speed is the calculated value when F_{ADC}=48MHz.

(2) When selecting reference voltage (+)=VDD, reference voltage (-)=V_{SS}

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V, reference voltage (+)=VDD, reference voltage (-)=V_{SS})

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	RES	-		-	12	-	bit
Combined error Note1	ET	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-	6	-	LSB
Zero scale error Note1	E_{ZS}	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-	0	-	LSB
Full scale error Note1	E_{FS}	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-	0	-	LSB
Integral linearity error Note1	EL	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-2	-	2	LSB
Differential linearity error Note1	ED	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-3	-	3	LSB
Conversion time Note3	T_{CONV}	12-bit resolution Conversion object: ANI0~ ANI15	2.0V≤VDD≤5.5V	45	-	-	1/F_{ADC}
		12-bit resolution Conversion object: internal reference voltage, temperature sensor output voltage, PGA output voltage	2.0V≤VDD≤5.5V	72	-	-	1/F_{ADC}
External input resistance	R_{AIN}	R_{AIN} <(T_S /(F_{ADC} x C_{ADC} x ln(2^{12+2}))- R_{ADC})		-	10^{Note4}	-	KΩ
Sampling switch resistance	R_{ADC}	-		-	-	1.5	KΩ
Sample-and-hold capacitance	C_{ADC}	-		-	2	-	pF
Analog input voltage	V_{AIN}	ANI0~ANI7		0	-	VDD	V
		ANI8~ANI15		0	-	VDD	V
		Internal reference voltage (2.0V≤VDD≤5.5V)		V_{BGR} Note2			V
		Temperature sensor output voltage (2.0V≤VDD≤5.5V)		V_{TMPS25} Note2			V

Note1: Quantization error (±1/2 LSB) is not included.

Note2: Please refer to “7. 8. 2 Characteristics of temperature sensor/internal reference voltage”.

Note3: F_{ADC} is the operation frequency of the AD, and the maximum operation frequency is 48MHz.

Note4: It is guaranteed by the design, and is not tested in mass production. The typical value is the default sampling period Ts=13.5, and the conversion speed is the calculated value when F_{ADC}=48MHz.

7.8.2 Characteristics of temperature sensor/internal reference voltage

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	V_{TMPS25}	T_A=25℃	-	1.09	-	V
Internal reference voltage	V_{BGR}	T_A= -40~10℃	1.25	1.45	1.65	V
		T_A=10~70℃	1.38	1.45	1.52	V
		T_A=70~125℃	1.35	1.45	1.55	V
Temperature coefficient	F_{VTMPS}	-	-	-3.5	-	mV/℃
Operation stabilization wait time	T_{AMP}	-	5	-	-	us

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

7.8.3 D/A converter

(T_A= -40~ 125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	RES	-	-	-	-	8	bit
Combined error	ET	Rload=4MΩ	2.0V≤VDD≤5.5V	-2.5	-	2.5	LSB
Stabilization time	T_{SET}	Cload=20pF	2.7V≤VDD≤5.5V	-	-	3	us
			2.0V≤VDD<2.7V	-	-	6	us
Output load	RO	Rload=4MΩ	2.0V≤VDD≤5.5V	4.7	-	8	KΩ

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

7.8.4 Comparator

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input offset voltage	V_{OFFSET}	-		-	±10	±40	mV
Input voltage range	V_{IN}	-		0	-	VDD	V
Internal reference voltage offset	ΔV_{IREF}	CmRVM register: 7FH~80H(m=0,1)		-	-	±2	LSB
		Others		-		±1	LSB
Response time	T_{CR}, T_{CF}	Input amplitude±100mV		-	70	125	ns
Operation stability time Note1	T_{STB}	CMPn=0->1	VDD =3.3~5.5V	-	-	1	us
			VDD =2.0~3.3V	-	-	3	
Reference voltage stabilization time	T_{VR}	CVRE=0->1Note2		-	-	20	us
Operating current	ICMPDD	See 7. 5. 2 Power supply current characteristics					

Note1: The time required from the comparator action enable (CMPnEN=0 ->1) to fulfill each DC/AC style requirement of the CMP.

Note2: After the internal reference voltage generator is enabled (by setting the CVREm bit to 1; m = 0 to 1), the comparator output can be enabled only after the reference voltage stabilization time has elapsed (CnOE bit = 1; n = 0 to 1).

Remark: It is guaranteed by the design, and is not tested in mass production.

7.8.5 Programmable gain amplifier (PGA)

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input offset voltage	V_{IOPGA}	-		-	±3	±10	mV
Input voltage range	V_{IPGA}	-		0	-	0.9xVDD/ Gain	V
Output voltage range	V_{IOHPGA}	-		0.93xVDD	-	-	V
	V_{IOLPGA}	-		-	-	0.07xVDD	V
Gain error	EG	x4	-	-	-	±1	%
		x8	-	-	-	±1	%
		x10	-	-	-	±1	%
		x12	-	-	-	±2	%
		x14	-	-	-	±2	%
		x16	-	-	-	±2	%
		x32	-	-	-	±3	%
Conversion rate Note2	SR_{RPGA}	Rising Vin= 0.1VDD/gain to 0.9VDD/gain. 10 to 90% of output voltage amplitude	4.0 V ≤VDD≤ 5.5 V (other than x32)	3.5	-	-	V/us
			4.0 V ≤VDD≤ 5.5 V(x32)	3.0	-	-	
			2.0 V ≤VDD≤ 4.0V	0.5	-	-	
	SR_{FPGA}	Falling Vin= 0.1VDD/gain to 0.9VDD/gain. 90 to 10% of output voltage amplitude	4.0 V ≤VDD≤ 5.5 V (other than x32)	3.5	-	-	
			4.0 V ≤VDD≤ 5.5 V(x32)	3.0	-	-	
			2.0 V ≤VDD≤ 4.0V	0.5	-	-	
Stable operation time Note1	T_{PGA}	x4	-	-	-	5	us
		x8	-	-	-	5	us
		x10	-	-	-	5	us
		x12	-	-	-	10	us
		x14	-	-	-	10	us
		x16	-	-	-	10	us
		x32	-	-	-	10	us
Operating current	I_{PGADD}	See 7. 5. 2 Power supply current characteristics					

Note1: The time required from the PGA action enable (PGAEN=1) to fulfill each of the DC and AC style requirements of the PGA.

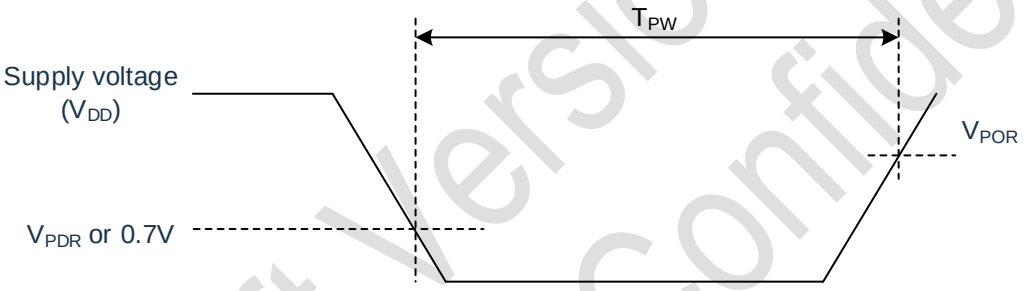
Note2: It is guaranteed by the design, and is not tested in mass production.

7.8.6 POR circuit characteristics

(T_A= -40~125°C, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detect voltage	V_{POR}	When the supply voltage rises	-	1.50	2.0	V
	V_{PDR}	When the supply voltage drops	1.37	1.45	-	V
Minimum pulse width Note1	T_{PW}	-	300	-	-	us

Note1: This is the time required to reset the POR when V_{DD} falls below V_{PDR}. In addition, when the oscillation of the main system clock (F_{MAIN}) is stopped by setting bit0 (HIOSTOP) and bit7 (MSTOP) of the clock operation status control register (CSC) in the deep sleep mode, this is the time required for POR reset from the time when V_{DD} is lower than 0.7V to the time when it rises above V_{POR}.



Remark: It is guaranteed by the design, and is not tested in mass production.

7.8.7 LVD circuit characteristics

(1) Reset mode, interrupt mode

(T_A= -40~125℃, V_{PDR}≤VDD≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection voltage	V_{LVD0}	When the supply voltage rises	-	4.06	4.26	V
		When the supply voltage drops	3.78	3.98	-	V
	V_{LVD1}	When the supply voltage rises	-	3.75	-	V
		When the supply voltage drops	-	3.67	-	V
	V_{LVD2}	When the supply voltage rises	-	3.02	-	V
		When the supply voltage drops	-	2.96	-	V
	V_{LVD3}	When the supply voltage rises	-	2.71	-	V
		When the supply voltage drops	-	2.65	-	V
	V_{LVD4}	When the supply voltage rises	-	2.09	2.16	V
		When the supply voltage drops	1.97	2.04	-	V
Minimum pulse width	T_{LW}	-	300	-	-	us
Detection delay	-	-	-	-	300	us

Remark: It is guaranteed by the design, and is not tested in mass production.

(2) Interrupt & reset mode

(T_A= -40~125℃, V_{PDR} ≤VDD≤5.5V, V_{SS}=0V)

Item	Symbol	Condition			Min.	Typ.	Max.	Unit
Interrupt & reset mode	V_{LVDB0}	V_{POC2}=0 V_{POC1}=0 V_{POC0}=1	Drop the reset voltage		1.78	1.84	-	V
	V_{LVDB2}		LVIS1=0 LVIS0=1	Rise the reset release voltage	-	2.09	2.16	V
				Drop the interrupt voltage	1.97	2.04	-	V
	V_{LVDC0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=0	Drop the reset voltage		-	2.45	-	V
	V_{LVDC2}		LVIS1=0 LVIS0=1	Rise the reset release voltage	-	2.71	-	V
				Drop the interrupt voltage	-	2.65	-	V
	V_{LVDC3}		LVIS1=0 LVIS0=0	Rise the reset release voltage	-	3.75	-	V
				Drop the interrupt voltage	-	3.67	-	V
	V_{LVDD0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=1	Drop the reset voltage		--	2.75	-	V
	V_{LVDD2}		LVIS1=0 LVIS0=1	Rise the reset release voltage	-	3.02		V
				Drop the interrupt voltage	-	2.96		V
	V_{LVDD3}		LVIS1=0 LVIS0=0	Rise the reset release voltage	-	4.06	4.26	V
				Drop the interrupt voltage	3.78	3.98	-	V

Remark: It is guaranteed by the design, and is not tested in mass production.

7.8.8 Rise slope characteristics of reset time and supply voltage

(T_A= -40~125℃, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time	T_{RESET}	-	-	1	-	ms
Rising slope of supply voltage	S_{VDD}	-	-	-	54	V/ms

Remark: It is guaranteed by the design, and is not tested in mass production.

7.9 LIN transceiver characteristics

7.9.1 Limit parameters

Item	Symbol	Test condition	Value	Unit
Supply voltage	V_{BAT}	To GND	-0.3 ~ +40	V
Pin voltage	V_{Cap}	To GND	-0.3~ +7	V
	V_{RXD}	To GND	-0.3~ V_{Cap} +0.3	V
	V_{EN}	To GND	-0.3~ V_{Cap} +0.3	V
	V_{RSTN}	To GND	-0.3~ V_{Cap} +0.3	V
	V_{TXD}	To GND	-0.3~ V_{Cap} +0.3	V
	V_{LIN}	To GND, to V_{BAT}	-40~ +40	V
Junction temperature	T_j	-	-40 ~ 150	℃
Storage temperature	T_{stg}	-	-55 ~ 150	℃

Caution: The maximum limit parameter value refers to a point beyond which the device may incur irreparable damage. Operating under these conditions is detrimental to normal device operation, and continuous operation at maximum rated values may affect device reliability. The reference point for all voltages is ground.

7.9.2 DC characteristics

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Power consumption						
Current consumption on V_{BAT} pin	I_{BAT}	Sleep mode: (V_{LIN}=V_{BAT})	-	10	-	μA
		Standby mode: (V_{LIN}=V_{BAT})	-	40	220	μA
		Normal mode (recessive): (V_{LIN}=V_{BAT}; V_{TXD}=V_{CC}; V_{RSTN}=HIGH)	-	200	600	μA
		Normal mode (dominant): (V_{BAT}=12V; V_{TXD}=0V; V_{RSTN}=HIGH)	-	2.5	4	mA
Power-on reset						
V_{BAT} power-down threshold voltage	$V_{th(BAT)L}$	-	3	-	4.7	V
V_{BAT} power-up threshold voltage	$V_{th(BAT)H}$	-	-	-	5.25	V
V_{BAT} hysteresis voltage	$V_{hys(BAT)}$	-	50	-	-	V
V_{Cap} pin						
Regulator output voltage	V_{CC}	$V_{Ccap(nom)}$ =5V; I_{Cap}=-70mA~0	4.9	5	5.1	V
Regulator output current limit	I_{Olim}	V_{Cap}=0 ~ 5.5V	-250	-	-70	mA
Power-down detection voltage	V_{UVD}	$V_{Cap(nom)}$ =5V	4.2	-	4.6	V
Power-down recovery voltage	V_{UVR}	$V_{Cap(nom)}$=5V	4.6	-	4.9	V
V_{BAT} to V_{Cap} resistance	$R_{(VBAT-Vcap)}$ [1]	$V_{Cap(nom)}$ = 5 V; V_{BAT}= 4.5V~ 5.5V I_{V1}= -70 mA~ -5mA	-	-	5	Ω
Output capacitance	C_O [1]	ESR < 5Ω	2.2	10	-	μF
TXD pin						
Input threshold voltage	$V_{th(SW)}$	V_{Cap} = 2.97V~5.5V	0.3V_{CC}	-	0.7V_{CC}	V
Input hysteresis voltage	$V_{hys(i)}$	V_{Cap} = 2.97V~5.5V	200	-	-	mV
Pull-up resistance	R_{pu}	-	5	12	25	kΩ
RXD pin						
Output current, high	I_{OH}	Normal mode V_{LIN} = V_{BAT}; V_{RXD} = V_{Cap}- 0.4V	-	-	-0.4	mA
Output current, low	I_{OL}	Normal mode V_{LIN} = 0; V_{RXD} = 0.4V	0.4	-	-	mA
EN pin						
Input threshold voltage	$V_{th(SW)}$	-	0.8	-	2	V
Pull-down resistance	R_{pd}	-	50	130	400	KΩ
RSTN pin						

Pull-up resistance	R_{pu}	$V_{RSTN}=V_{Cap}$-0.4V V_{Cap}=2.97V~5.5V	3	-	12	kΩ
Output current, low	I_{OL}	V_{RSTN}=0.4V V_{Cap} =2.97V~5.5V -40℃<Tj<195℃	3.2	-	40	mA
Output voltage, low	V_{OL}	V_{Cap}=2.5V~5.5 V -40℃<Tj<195℃	0	-	0.5	V
Output voltage, high	V_{OH}	-40℃<Tj<195℃	0.8V_{CC}	-	V_{CC}+0.3	V
LIN pin						
Driver dominant current limit	I_{BUS_LIM}	V_{TXD}=0V; $V_{LIN}=V_{BAT}$=18V	40	-	100	mA
Receiver recessive input leakage current	$I_{BUS\_PAS\_rec}$	$V_{TXD}=V_{cap}$; V_{LIN}=18V; V_{BAT}=5.5V	-	-	20	μA
Receiver dominant input leakage current	$I_{BUS\_PAS\_dom}$	Normal mode; $V_{TXD}=V_{cap}$; V_{LIN}=0V; V_{BAT}=12V	-1000	-	-	μA
Bus to Ground leakage current	$IL_{(log)}$	V_{BAT}=18V; VLIN=0V	-1000	-	10	μA
Bus to power leakage current	$IL_{(lob)}$	V_{BAT}=0V; VLIN=18V	-	-	20	μA
Receiver dominant flip-flop threshold voltage	$V_{th(dom)RX}$	V_{BAT}=5.5V~18V	-	-	0.4V_{BAT}	V
Receiver recessive flip-flop threshold voltage	$V_{th(rec)RX}$	V_{BAT}=5.5V~18V	0.6V_{BAT}	-	-	V
Receiver center flip threshold voltage	$V_{th(RX)cntr}$	V_{BAT}=5.5V~18V $V_{th(RX)\ cntr}$= ($V_{th(rec)RX}$ + $V_{th(dom)RX}$)/2	0.475V_{BAT}	0.5V_{BAT}	0.525V_{BAT}	V
Receiver hysteresis threshold voltage	$V_{th(hys)RX}$	V_{BAT}=5.5V~18V $V_{th(hys)RX}=V_{th(rec)RX}$ - $V_{th(dom)RX}$	-	-	0.175V_{BAT}	V
Slave resistance	R_{slave}	Equivalent resistance between LIN and V_{BAT}; V_{LIN} = 0V; V_{BAT}=12V	20	30	60	KΩ
LIN pin equivalent capacitance	C_{LIN} [1]	-	-	-	30	pF
Dominant output voltage	$V_{o(dom)}$	Normal mode; V_{TXD}=0V; V_{BAT}=7V	-	-	1.4	V
		Normal mode; V_{TXD}=0V; V_{BAT}=18V	-	-	2.0	V
Thermal shutdown						
Shutdown junction temperature	$T_{j(sd)}$ [1]	-	150	180	200	℃

(If not otherwise specified, 5.5V ≤ V_{BAT} ≤ 28V, -40°C ≤ T_j ≤ 150°C, typical at V_{BAT} = 12V, T_j = 25°C.)

[1] Design value guaranteed, not test result.

7.9.3 Switching characteristics

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Duty cycle						
Duty cycle 1	δ1 [1][2]	Vth(rec)(max)=0.744×VBAT; Vth(dom)(max)=0.581×VBAT; t_{bit}=50μs; V_{BAT}=7V~18V	0.396	-	-	-
		Vth(rec)(max)=0.76×VBAT; Vth(dom)(max)=0.593×VBAT; t_{bit}=50μs; V_{BAT}=5.5V~7V	0.396	-	-	-
Duty cycle 2	δ2 [2][3]	Vth(rec)(min)=0.422×VBAT; Vth(dom)(min)=0.284×VBAT; t_{bit}=50μs; V_{BAT}=7.6V~18V	-	-	0.581	-
		Vth(rec)(min)=0.41×VBAT; Vth(dom)(min)=0.275×VBAT; t_{bit}=50μs; V_{BAT}=6.1V~7.6V	-	-	0.581	-
Duty cycle 3	δ3 [1][2]	Vth(rec)(max)=0.778×VBAT; Vth(dom)(max)=0.616×VBAT; t_{bit}=96μs; V_{BAT}=7V~18V	0.417	-	-	-
		Vth(rec)(max)=0.797×VBAT; Vth(dom)(max)=0.630×VBAT; t_{bit}=96μs; V_{BAT}=5.5V~7V	0.417	-	-	-
Duty cycle 4	δ4 [2][3]	Vth(rec)(min)=0.389×VBAT; Vth(dom)(min)=0.251×VBAT; t_{bit}=96μs; V_{BAT}=7.6V~18V	-	-	0.590	-
		Vth(rec)(min)=0.378×VBAT; Vth(dom)(min)=0.242×VBAT; t_{bit}=96μs; V_{BAT}=6.1V~7.6V	-	-	0.590	-
Timing characteristics						
Receiver propagation delay	$t_{PD(RX)}$ [4]	-	-	-	6	μs
Receiver propagation delay symmetry	$t_{PD(RX)sym}$ [4]	-	-2	-	2	μs
Dominant wake-up time for LIN (remote wake-up)	$t_{wake(dom)LIN}$	Sleep mode	30	65	150	μs
Dominant wake-up time for WAKE_N (local wakeup)	$t_{wake(dom)WAKE\_N}$	Sleep mode	7	22	50	μs
Normal mode entry time	$t_{gotonorm}$	-	2	5	10	μs
Sleep mode entry time	$t_{gotosleep}$	-	2	5	10	μs
TXD dominant timeout time	$t_{to(dom)TXD}$	V_{TXD}=0V	27	52	90	ms

(If not otherwise specified, 5.5V≤V_{BAT}≤27V, -40°C≤T_{vj}≤150°C, typical at V_{BAT}=12V, T_{vj}=25°C.)

1) δ1, δ3=$\frac{t_{bus(rec)(min)}}{2\times t_{bit}}$

2) Bus load: (1) C_L=1nF, R_L=1kΩ; (2) C_L=6.8nF, R_L=660Ω; (3) C_L=10nF, R_L=500Ω

3) δ2, δ4=$\frac{t_{bus(rec)(max)}}{2\times t_{bit}}$

4) Receiver output pin RXD load condition: C_{TXD}=20pF, R_{RXD}=2.4kΩ

7.10 Memory characteristics

7.10.1 Flash memory

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Symbol	Item	Condition	Min.	Max.	Unit
T_{PROG}	Word program(32-bit)	T_A= -40~125℃	24	30	us
T_{ERASE}	Sector erase	T_A= -40~125℃	4	5	ms
	Chip erase	T_A= -40~125℃	20	40	ms
N_{END}	Endurance	T_A= -40~125℃	100	-	kcycle
T_{RET}	Data retention	100 kcycle Note1 at T_A =125℃	20	-	Years

Note1: Cycling tests are performed over the entire temperature range.

Remark: It is guaranteed by the design, and is not tested in mass production.

7.10.2 RAM memory

(T_A= -40~125℃, 2.0V≤VDD≤5.5V, V_{SS}=GND=0V)

Symbol	Item	Condition	Min.	Max.	Unit
$V_{RAMHOLD}$	RAM hold vltage	T_A= -40~125℃	0.8	-	V

Remark: It is guaranteed by the design, and is not tested in mass production.

7.11 EMS characteristics

7.11.1 ESD eletrical characteristics

Symbol	Item	Test condition	Grade
$V_{ESD(HBM)}$	Electrostatic discharge (Human-Body Model HBM)	T_A = 25°C, JEDEC EIA/JESD22- A114	3A

Remark: It is guaranteed by the design, and is not tested in mass production.

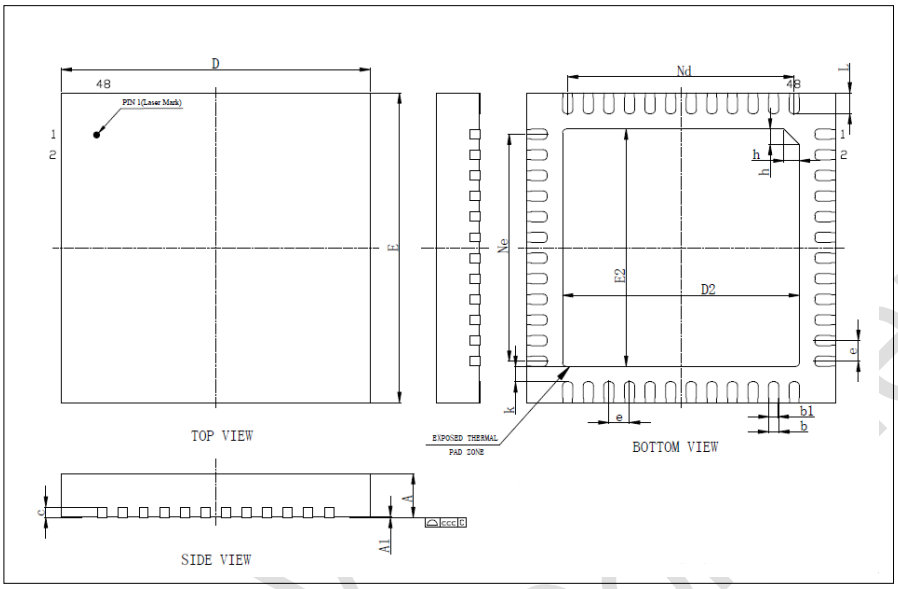
7.11.2 Latch-up electrical characteristics

Symbol	Item	Test condition	Classification
LU	Static latch-up class	JEDEC STANDARD NO.78E NOVEMBER 2016	Class II A (T_A = 125°C)

Remark: It is guaranteed by the design, and is not tested in mass production.

8 Package

8.1 QFN48 (6x6mm, 0.4mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1		0.18REF	
c		0.203REF	
D	5.90	6.00	6.10
D2	4.55	4.60	4.65
e		0.40BSC	
Nd		4.40BSC	
Ne		4.40BSC	
E	5.90	6.00	6.10
E2	4.55	4.60	4.65
L	0.35	0.40	0.45
h	0.25	0.30	0.35
R		0.075REF	
k	0.25	0.30	0.35

9 Revision History

Version	Date	Revision content
V0.1.0	November 2023	Initial version
V0.1.1	January 2024	1) Revised Product Structure Diagram 2) Added current parameters in Section 7.3 3) Revised 1.2/1.3.1/5.1.1/5.2/7.2/7.3/7.5.1/7.5.2
V0.1.2	April 2024	1) Revised 7.1 Typical application peripheral circuits 2) Revised Vcap function description
V0.1.3	April 2024	1) Corrected 2 Product Structure Diagram 2) Updated Sections 1.1/6.1